CMOS ΔΣAD Modulators using Dynamic Analog Components

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Abstract: CMOS ΔΣAD modulator using dynamic analog components for low power and high signal to noise and distortion (SNDR) application is presented. The proof-of-concept CMOS ΔΣAD modulators using dynamic analog components are designed and fabricated in 90nm CMOS technology. The integrators in the modulator are realized by dynamic amplifiers without static current. Successive approximation register (SAR) quantizer in the modulator is realized by a passive capacitor array and a dynamic comparator. The dynamic analog components do not dissipate the static power at all. Measurement results of the experimental prototype ΔΣADCs demonstrate the feasibility and reliability of the proposed techniques. Peak SNDR=77.93dB and SNR=84.16dB are achieved while a sinusoid -4dBFS input is sampled at 14MS/s with the bandwidth of BW=109kHz. The total analog power consumption of the prototype modulator is 420µW with the supply voltage of 1.1V.

I. Introduction

High SNDR ADCs are widely used in mixed-signal SoC in the fields of both the consumer and industrial applications. The SAR ADC is well known as an energy efficiency architecture for low and medium-speed, medium-resolution applications [1], [2]. However, because the resolution of SAR ADC depends on accuracy of capacitor matching and offset of comparator, it is difficult to realize high resolution SAR ADC in nanoscale CMOS technology. On the other hand, the ΔΣAD modulator reduces the quantization noise in the desired signal band using the oversampling and noise-shaping technique. Thus, it is suitable to realize the high SNDR ADC in nanometer CMOS technology [3]. The high SNDR modulator is realized by the technique of high-order noise-shaping, and normally, high-order integrators with power hungry amplifiers.

In order to achieve the maximum power-efficiency of the amplifier in the ADC, the use of the dynamic amplifier (e.g., logic inverter or ring amplifier) instead of operational-transconductance-amplifier (OTA) has been proposed, which is called the dynamic-analog-components-based ADC [4], [5]. The drawback of using the dynamic component is that it needs the reset operation which limits the conversion speed of the ADC. This paper proposes a ΔΣAD modulator architecture with ring amplifier and passive adder embedded SAR quantizer. Measurement results of the proposed prototype ΔΣAD modulators demonstrate the feasibility and reliability of the proposed techniques. Measurement results of improved prototype show that the experimental ΔΣAD modulator can guarantee the reset time for ring amplifier and relax the speed requirement on the asynchronous SAR quantizer.

II. Proposed ΔΣAD Modulator Architecture

A. Architecture 1

Fig. 1 shows the block diagram of conventional 2nd-order feed-forward ΔΣAD modulator using SAR quantizer and ring amplifier [6]. The switched-capacitor integrator of ΔΣAD modulator is realized by the ring amplifier. The operation of ring

Fig. 1. Block diagram of the 2nd-order feed-forward ΔΣAD modulator using SAR ADC and ring amplifier [6].
amplifier is different from that of the traditional amplifier. The ring amplifier needs to operate alternately between the reset mode and amplification mode. Since the output of ring amplifier is disabled at the reset mode, the load capacitance must be connected to the output of the ring amplifier at the amplification mode. Furthermore, since SAR ADC is used as an internal quantizer in ΔΣAD modulator, unlike flash ADC, SAR ADC must use an extra phase for sampling operation. Due to the constraint of the above two factors, the clock timing design of ΔΣAD modulator using SAR ADC and ring amplifier is more difficult than the ΔΣAD modulator using traditional amplifier and flash ADC. Considering the above factors, in order to correctly implement the transfer function of conventional 2nd-order feed-forward ΔΣAD modulator, the ΔΣAD modulator must be designed according to Fig. 2(a) and Fig. 2(b). Fig. 2(a) shows the circuit implementation of ΔΣAD modulator using SAR ADC and ring amplifier(R-AMP), and its timing diagram is shown in Fig. 2(b). Because the ΔΣAD modulator needs to operate in 4-phase, it is complicated and the speed of operation is limited.

The 2nd-order ΔΣAD modulator is designed and fabricated in the TSMC 90nm 1P9M CMOS technology without any option for precision capacitors and low threshold voltages. Fig. 3 shows a microphotograph of the experimental prototype and the layout of the ΔΣAD modulator. The active area of the ΔΣAD modulator is 610μm × 254μm. Fig. 4 shows the measured output power spectrum of the prototype modulator for a 5.493kHz sinusoid differential -1dBFS input sampled at 12MS/s. The peak SNDR=77.51dB is achieved for 94kHz bandwidth (OSR=64). Fig. 5 shows the measured SNR and SNDR vs. input signal level. Peak SNDR of 77.51dB and SNR of 80.08dB at -1.1dBFS are achieved, respectively. The measurement results of the modulator show that linear SNDR response up to the full scale, and the dynamic range of 84dB is achieved. The total power consumption of this work is 0.37mW. Both the analog and digital circuits supply voltage is 1.1V. The Schreier and Walden FOMs are 161.5dB and 0.32pJ/conversion-step, respectively. Measurement results show the reliability of ΔΣAD modulator with dynamic analog components.

B. Architecture 2

To simplify the operation phase of the ΔΣAD modulator for improving the speed of the ΔΣAD modulator, we propose the ΔΣAD modulator architecture as shown in Fig. 6 that allows the ΔΣAD modulator to work in 3-phase. The operation of the proposed modulator can be completed in 3-phase, so that the speed of modulator can be improved. Although the operation timing
Fig. 3. Chip microphotograph and layout of the prototype modulator.

Fig. 4. Measured output spectrum for \( f_{\text{in}} = 26.92 \text{kHz} \) and \(-4\text{dBFS}\) input signal amplitude.

Fig. 5. Measured results of SNDR and SNR vs. input signal level [dBFS]

Fig. 6. The improved architecture of the \( \Delta \Sigma \) AD modulator.

Fig. 7. Circuit implementation of the proposed \( \Delta \Sigma \) modulator using SAR quantizer and ring amplifier with simplified operation phases. (a) Circuit schematic diagram. (b) Clock timing chart.
of these two kinds of \( \Delta \Sigma \text{AD} \) modulator(Fig. 1 and Fig. 6) are different, the architecture of the proposed \( \Delta \Sigma \text{AD} \) modulator(Fig. 6) can still realize the 2nd-order noise sharpening transfer characteristic that can be proved as the following.

In Fig. 6, \( u(n) \) is the input, and \( v(n) \) is the output of the \( \Delta \Sigma \text{AD} \) modulator. The input signal of the 4bit sub-ADC in Fig. 1 is given as

\[
y(n) = u(n) + 2x_1(n) + x_2(n),
\]

where \( x_1(n) \) is the output signal of the 1st integrator , \( x_2(n) \) is the output signal of the 2nd integrator.

Since the output signal of the 2nd integrator obey the following relationship

\[
x_2(n+1) = x_1(n) + x_2(n)
\]

by combining it with (1) and (2) will lead to

\[
y(n) = u(n) + x_1(n) + x_2(n + 1)
\]

Consequently, the \( \Delta \Sigma \text{AD} \) modulator in fig. 1 can be changed to that shown in fig. 6. The output signal of the \( \Delta \Sigma \text{AD} \) modulator shown in fig. 6 is obtained as

\[
v(n) = u(n) + q(n) + x_1(n) + x_2(n + 1).
\]

The z-domain expression of Eq.(4) can be written as

\[
V(z) = U(z) + Q(z) + X_1(z) + X_2(z)z.
\]

In fig. 6 the z-domain expression of the 1st and the 2nd integrator’s output signal are given as

\[
X_1(z) = \frac{U(z) - V(z)}{1 - z^{-1}}
\]

\[
X_2(z)z = \frac{X_1(z)}{1 - z^{-1}}
\]

Substituting Eq.(6) and (7) into Eq.(5) we get

\[
V(z) = U(z) + (1 - z^{-1})^2Q(z)
\]

The transfer function of the proposed \( \Delta \Sigma \text{AD} \) modulator expressed in Eq.(8) shows the 2nd-order noise sharpening characteristic. It is the same as that in Fig. 1. The equivalence of two kinds of the \( \Delta \Sigma \text{AD} \) modulator architecture(Fig. 1 and Fig. 6) can be confirmed. However, only three operation phases are required in the proposed \( \Delta \Sigma \text{AD} \) modulator, so that the operation speed of modulator can be improved.
III. IMPROVED ΔΣAD MODULATOR IMPLEMENTATION

Fig. 7(a) shows the circuit schematic diagram of the proposed 2nd-order ΔΣAD modulator using SAR ADC and ring amplifier with simplified operation phase with its clock timing chart shown in Fig. 7(b). Because the signal \( V_U \) and \( V_o2 \) are sampled during the same phase by SAR quantizer as shown in Fig. 7(a), in contrast to Fig. 1(b), the conversion of the proposed ΔΣAD modulator can be completed in three phases. The ΔΣAD modulator operation mode can be simplified. In addition, a high-speed SAR ADC is used as a 4-bit quantizer. It not only improves the stability of the modulator, but also relaxes the requirement on the slew-rate of amplifier. The 4-bit SAR ADC has 3 inputs terminal (\( V_U \), \( V_o1 \) and \( V_o2 \)), benefit from the SAR ADC converting the summation of them to digital code, the analog adder is realized by capacitor array without amplifier. Moreover, the ring amplifier does not need static current, so that the power consumption can be maintained low.

A. SAR ADC with Passive Adder

Fig. 8 shows the schematic of the proposed SAR ADC with embedded adder. In the sampling mode, the bottom plate of the sampling capacitors are connected to input signals of \( V_U \), \( V_o1 \) and \( V_o2 \) and the top plate sampling capacitors are connected to \( V_{cm} \), the capacitor ratio for 3 input signals is 1:1:1. In the successive approximation converting mode, the bottom plates of the sampling capacitors are connected to \( V_{cm} \). According to charge conservation law, the input voltage of the comparator \( V_x \) can be expressed as:

\[
V_x = \frac{V_U + V_o2 + V_o1}{3}
\]  

Equation (9) means that the summation of 3 input signals can be realized by the proposed sampling technique with capacitor array. After the analog input summation finished, the AD conversion will be carried out from MSB to LSB as same as a conventional SAR ADC does. As above mentioned, the proposed SAR ADC realizes not only a 4-bit quantizer but also an analog adder with the capacitor array and a comparator.

B. Pseudo Differential Ring Amplifier

In this work, we use the pseudo differential ring amplifier to realize the integrator and reduce the power consumption of modulator. Fig. 9(a) shows the pseudo differential ring amplifier and common mode feedback (CMFB) structure. \( C_{CS} \) are added to the input nodes of the amplifier to realize the amplifier input offset cancellation for the integrator [5]. Fig. 9(b) shows the schematic of the ring amplifier’s core in the proposed ΔΣAD modulator. It is constructed with three cascaded stage inverters. The input of the MOSFET \( M_{P1} \) and \( M_{N1} \) are biased at \( V_{cm} \) when the ring amplifier forms a feedback loop, therefore, the \( M_{P1} \) and \( M_{N1} \) operate in the weak inversion region during the steady state of the amplifier with a very low static current. The inverter which consists of \( M_{P1} \) and \( M_{N1} \) behaves as a class-AB amplifier providing high DC-gain and good linearity. Resistor \( R_{OS} \) is inserted to the output of the 2nd stage inverter. The \( R_{OS} \) can compress the drain-source voltage of \( M_{P2} \) and \( M_{N2} \) to...
the boundary between the weak and strong inversion regions for obtaining both high DC-gain and wide GB[4]. In addition, it also generates the different offset voltages to the gate of the $M_{P3}$ and $M_{N3}$ for setting their gate-source voltage less than their threshold voltage, thus $M_{P3}$ and $M_{N3}$ are cut off during the steady state of the amplifier without static current, the power consumption of the ring amplifier can be reduced. One of the two transistors $M_{P3}$, $M_{N3}$ is operating in the strong inversion region while the other is completely off during transition providing at a high slew rate, thus the setting time of the ring amplifier can be reduced dramatically. The push-pull inverter which consists of $M_{P3}$ and $M_{N3}$ behaves as a class-C amplifier and the rail-to-rail output is allowed for the ring amplifier. Because the input referred noise of SC integrator using the ring amplifier depends on the class-AB amplifier which consists of $M_{P1}$ and $M_{N1}$ mainly, the power of the input referred noise is obtained as

$$\frac{GB}{f_s} \times \frac{4kT}{3g_m} \approx \frac{20kT}{3g_m}$$ \hspace{1cm} (10)

where the ratio of the unit-gain-bandwidth(GB) and the sampling frequency($f_s$) is set as 5 in the $\Delta\Sigma$ AD modulator. The noise level of a ring-amplifier-based SC integrator is better than the thermal noise of a conventional SC integrator using an OTA[4]. Moreover, high threshold voltage $M_{P2,3}$ and $M_{N2,3}$ are used in the 2nd,3rd-stage to extend the stable offset voltage range for the amplifier.

IV. MEASUREMENT RESULTS

The improved $\Delta\Sigma$ AD modulator was fabricated in TSMC 90nm 1P9M CMOS technology. Fig. 10 shows the chip microphotograph and layout of the $\Delta\Sigma$ AD modulator. The active area of the $\Delta\Sigma$ AD modulator is 0.14mm². Fig. 11 shows the measured output power spectrum of the prototype modulator for a 26.92kHz sinusoid differential -4dBFS input signal amplitude. Due to the influence of the bootstrapped switch’s nonlinearity, when a full dynamic range signal is inputted, the 3rd-order harmonics distortion imposes some performance issue that is verified by the SPICE simulation. Fig. 12 shows the measured SNR and SNDR vs. input signal level. Peak SNDR of 77.93dB and SNR of 84.16dB at -1.24dBFS and -4.37dBFS are achieved, respectively. The measurement results of the modulator show that linear SNDR responses up to the full scale, and the dynamic range of 85dB is achieved. The total power consumption of this work is 420$\mu$W. Both analog and digital circuits supply voltage are 1.1V. The Schreier FOM$_{SNDR}$ is 162.1dB. The performance of the improved $\Delta\Sigma$ AD modulator is summarized in Table I in comparison with the previous works.

V. CONCLUSIONS

Improved 2nd-order $\Delta\Sigma$ AD modulator with simplified operation mode using ring amplifier and asynchronous SAR ADC has been designed and fabricated in 90nm CMOS technology. Benefit from the reduction of the number of the $\Delta\Sigma$ AD modulator operation mode, comparing with the previous work [6], the speed and bandwidth of the $\Delta\Sigma$ AD modulator with simplified operation mode are improved by 16.7% ((14-12)/12=16.7%) for the proximate performance level (FOMW and FOMS). Moreover, the pseudo differential amplifier based ring amplifier is used for extending the dynamic range of the modulator.
for higher SNDR, and the SAR quantizer with the passive-adder is used, instead of quantizer and active adder. The ΔΣAD modulator circuit is realized by dynamic analog component, therefore the power consumption can be kept at low level. Measurement results show the feasibility of the proposed ΔΣAD modulator. This work is supported by VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

**REFERENCES**


