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Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Grounded Field Plate

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Abstract. We proposed a 0.18 μm CMOS compatible dual RESURF 40 V N-LDMOS transistor with a grounded field plate for automotive applications, which showed a wide SOA, high hot carrier endurance, low specific on-resistance, and low switching loss. However, the previous work did not adequately assess switching loss. Thus, we have analyzed the switching characteristics of the proposed device in detail by changing the load resistance R_L and the gate resistance R_G. TCAD simulations verified that under actual use conditions, the total energy loss (the total switching loss and the conduction loss) of the proposed device is sufficiently lower than that of the conventional one whose field plate connects to the gate. The lowest ratio of the total energy loss of the proposed device to that of the conventional one is 0.31 at a switching frequency of 3 MHz and a duty ratio of 0.1. This lowest value is because although the output capacitance of the proposed device is higher than that of the conventional ones, the feedback capacitance of the proposed device is considerably lower than that of the conventional ones.

1. Introduction

Switches of power converters in integrated circuits for automotive applications require high-performance Lateral Double Diffused MOS (LDMOS) transistors. To meet requirements from automotive applications, we proposed a 0.18 μm CMOS compatible dual REduced SURface Field (RESURF) 40 V N-LDMOS transistor with a grounded field plate [1,2]. The proposed device has a wide Safe Operating Area (SOA) and high hot carrier endurance due to the dual RESURF structure and the field plate. In addition, compared with a conventional LDMOS transistor whose field plate connects to the gate, the proposed device showed a much lower figure of merit (FOM) of switching loss, $R_{on,sp} \times Q_G$ (specific on-resistance times gate charge), mainly due to a much lower Miller effect caused by the grounded field plate. In this previous work, however, we evaluated the switching loss only under one condition. Since it needs to investigate under many conditions by considering actual use, a detailed evaluation of the switching loss is required.

In this paper, therefore, we have analyzed the switching characteristics of the proposed device in detail by changing the load resistance R_L and the gate resistance R_G as shown in Fig. 1 using the device

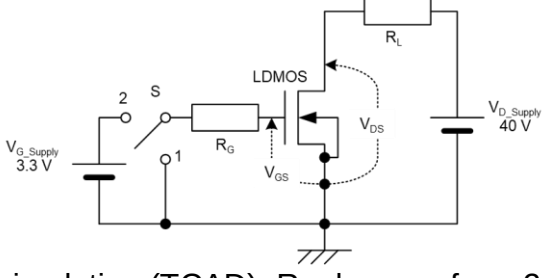


Fig. 1. Circuit for device simulation (TCAD). R_L changes from 2.13 Ωmm^2 to 10.7 Ωmm^2, and R_G, from 1.07 Ωmm^2 to 5.33 Ωmm^2 for a unit LDMOS layout area of 1 mm^2.

simulator in 3D TCAD developed by AdvanceSoft Corporation [3].

2. Device Structures and Features

Fig. 2 shows rough cross-sectional views of the conventional and the proposed LDMOS transistors. The structure inside the silicon of both devices is the same. Two P-type buried layers, PBL1 and PBL2, for both devices form a dual RESURF structure which reduces the electric field in the drift region adequately. The difference between both devices is how the field plate is connected. The field plate in the conventional device connects to the gate, while one in the proposed device, to the ground. Therefore, the proposed device has a much lower Miller capacitance than the conventional device, leading to a lower switching loss. The specific on-resistance of the conventional and the proposed devices is 39.8 $m\Omega mm^2$ and 40.8 $m\Omega mm^2$, respectively. This lower on-resistance of the former device is due to the field plate connected to the gate, which reduces the resistance in the drift region in the on-state. The extrapolated threshold voltage of the conventional and the proposed devices is the same, 1.05 V.

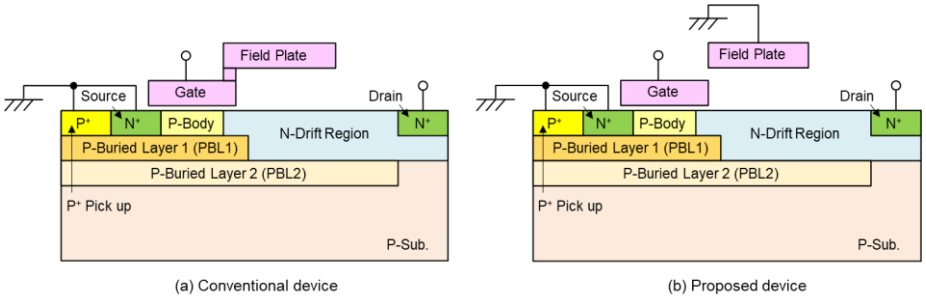


Fig. 2. Rough cross-sectional views of the conventional and the proposed devices.

3. Simulation Results

3.1 Turn-on Process

Fig. 3 shows turn-on characteristics of the conventional and the proposed devices. Turn-on characteristics of the former device divide into four regions (See Fig. 3 (a)). Region A is in the off-state due to the gate-source voltage V_{GS} less than the threshold voltage V_T where V_{GS} increases and the gate current I_G, the gate current density J_G, flows, charging the input capacitance (C_{GS}), the feedback capacitance (the Miller capacitance: C_{GD}+C_{FD}), and the output capacitance (C_D) (See Table 1 for the capacitances). Region B is in the gate plateau state due to charging C_{GD}+C_{FD} where the drain-source voltage V_{DS} decreases and the drain current density J_D increases, causing a long and intense Miller effect and discharging C_D (See Fig. 4 (a)). Region C is also in the gate plateau state, but the RESURF effect in the gate-side drift region around the drain of the intrinsic MOSFET disappears in this region, leading to a steep decrease in the drain voltage of the intrinsic MOSFET V_{DS_INT}. Region D is in the on-state.

Turn-on characteristics of the proposed device divide into four regions (See Fig. 3 (b)). Region A is in the off-state due to $V_{GS} < V_T$ where V_{GS} increases and I_G flows, charging the input capacitance (C_{GS}+C_{FG}), the feedback capacitance (C_{GD}), and the output capacitance (C_D+C_{FD}) (See Table 1 for the capacitances). Region B is in the J_D increasing and V_{DS} decreasing state with increasing V_{GS}, where the increase in the displacement current density (J_{FP}+J_{PB}+J_{Sub}) due to discharging C_D+C_{FD} causes a gradual decrease in V_{DS_INT}. Therefore, C_{GD} mainly charges by increasing V_{GS}, resulting in a weak Miller effect (See Fig. 4 (b)). Region C is in the gate plateau state, or a convex-shape gate plateau state, due to charging C_{GD} caused by a steep decrease in V_{DS_INT}, indicating a short but slightly intense Miller effect. This decrease is because the RESURF effect in the gate-side drift region around the drain of the intrinsic MOSFET disappears. Region D is in the on-state. The characteristics of V_{DS} and J_D in Regions

B and C of the proposed device are significantly different from those of the conventional device. This difference is because the field plate of the proposed device is the output capacitance, while that of the conventional one is the feedback capacitance.

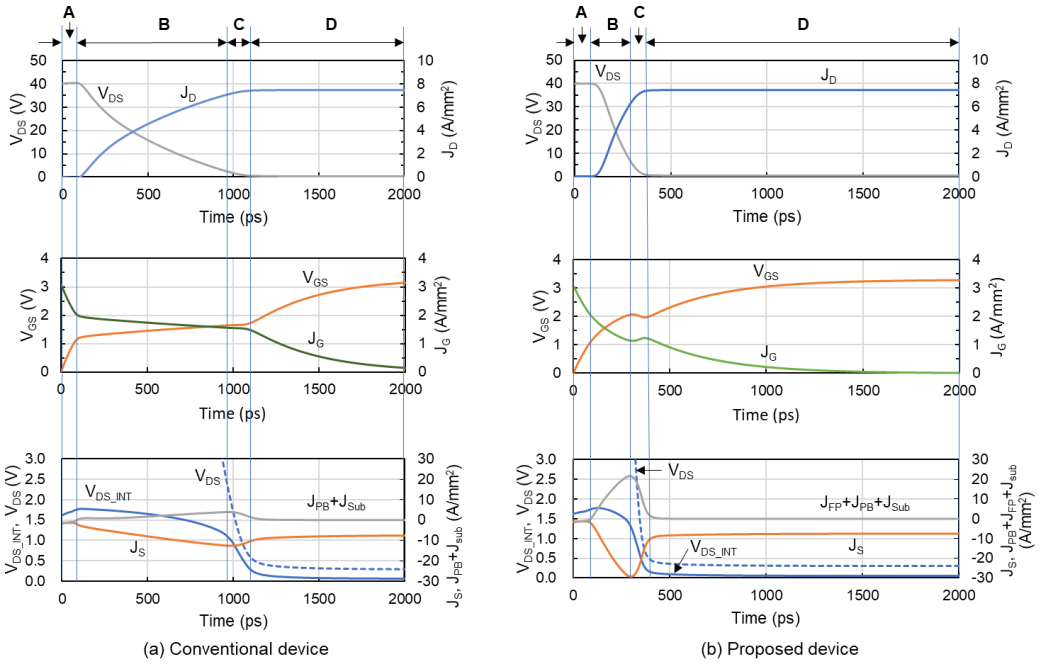


Fig. 3. Changes in turn-on characteristics with time at a low R_G of 1.07 Ωmm^2 and a middle R_L of 5.33 Ωmm^2 with a unit LDMOS layout area of 1 mm^2. The above characteristics are similar to those obtained under other conditions simulated in this paper.

Table 1. Parasitic capacitances in the LDMOS transistor. C_{GC} practically works when $V_{GS} > V_T$.

Capacitance	Conventional	Proposed
Input capacitance	$C_{GS}+C_{GC}$	$C_{GS}+C_{GC}+C_{FG}$
Feedback capacitance	$C_{GD}+C_{FD}$	C_{GD}
Output capacitance	C_D	C_D+C_{FD}

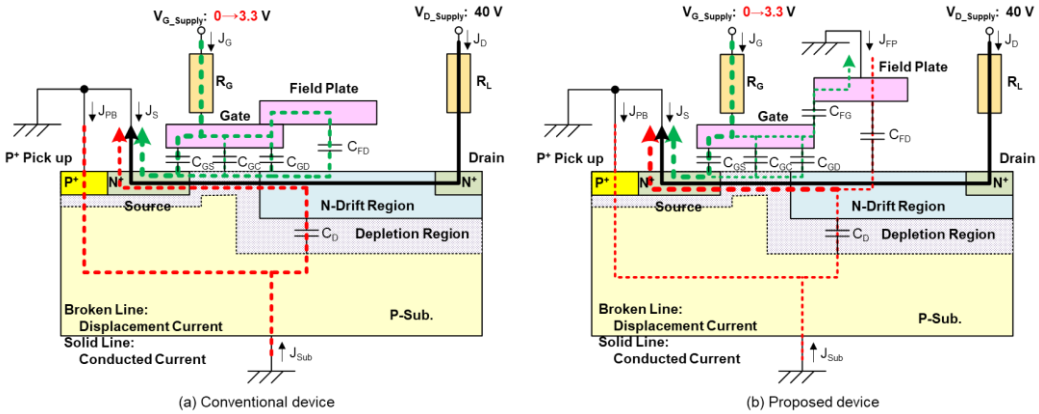
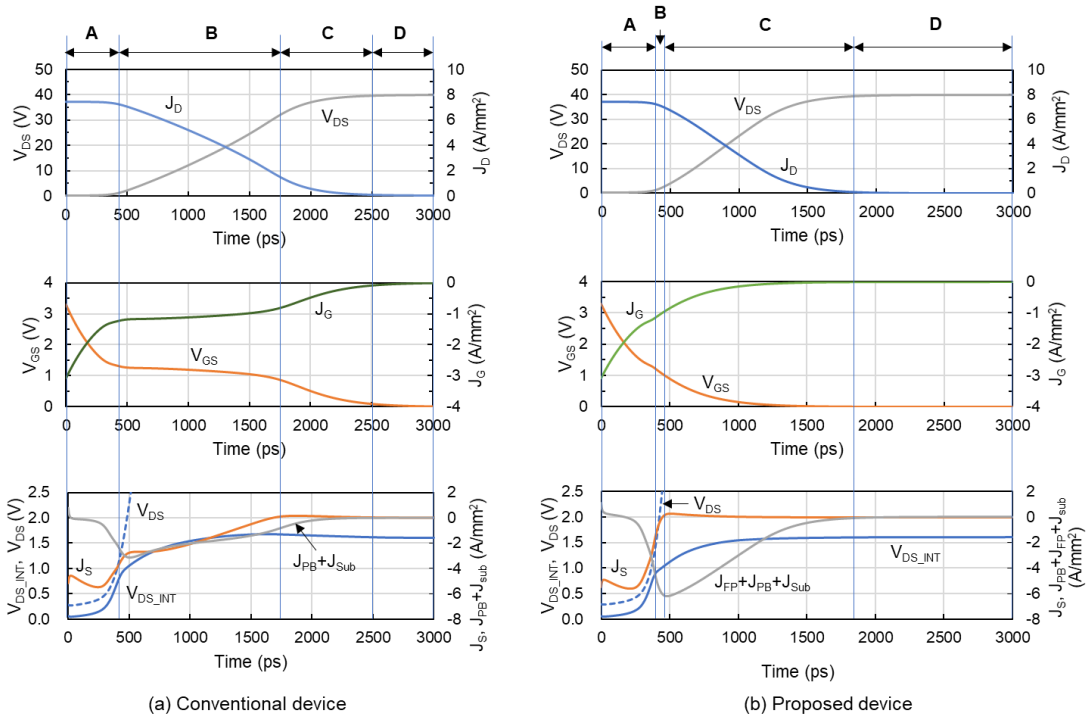


Fig. 4 Current paths for turn-on process when $V_{GS} > V_T$. After V_{GS} attaining the gate supply voltage V_{G_Supply}, displacement currents through parasitic capacitances disappear, and the conduction current from the drain to the source leaves.

3.2 Turn-off Process

Fig. 5 shows turn-off characteristics of the conventional and the proposed devices. The turn-off process takes much longer than the turn-on process. Turn-off characteristics of the former device divide into four regions (See Fig. 5 (a)). Region A is in the on-state due to $V_{GS} > V_T$ where V_{GS} decreases and $|J_G|$ also decreases, discharging the input capacitance (C_{GS}+C_{GC}) and the feedback capacitance (C_{GD}+C_{FD}), and then the increase in V_{DS_INT} and V_{DS} charges the output capacitance (C_D). At the end of Region A, the RESURF effect occurs in the gate-side drift region around the drain of the intrinsic MOSFET. Region B is in the gate plateau state where V_{DS} increases and J_D decreases, charging C_D and C_{GD}+C_{FD}; charging C_{GD}+C_{FD} causes a long and intense Miller effect (See Fig, 6 (a)). Region C is in the off-state of the intrinsic MOSFET due to almost no source current density J_S, where V_{DS} still increases, charging C_D and C_{GD}+C_{FD}. Region D is in the off-state.

Turn-off characteristics of the proposed device divide into four regions (See Fig. 5 (b)). Region A is in the on-state due to $V_{GS} > V_T$. The process of this region is almost similar to that of the conventional device. Here, the decrease in V_{GS} discharges the input capacitance (C_{GS}+C_{GC}+C_{FG}) and the feedback capacitance (C_{GD}), and the increase in V_{DS_INT} and V_{DS} charges the output capacitance (C_D+C_{FD}) mainly. At the end of Region A, the RESURF effect occurs in the gate-side drift region around the drain of the intrinsic MOSFET. Region B is in the beginning stage of turn-off due to $V_{GS} \gtrsim V_T$, where V_{DS} starts to increase and J_D decrease. In this region, a slight increase in V_{DS_INT} and a slight decline in V_{GS} cause a short and weak Miller effect, not gate plateau observed, and the displacement current density (J_{FP}+J_{PB}+J_{Sub}) charges the output capacitance (C_D+C_{FD}) (See Fig. 6 (b)). Region C is in the off-state of the intrinsic MOSFET due to almost no source current density J_S, where V_{DS} increases significantly, charging C_D+C_{FD} mainly. Region D is in the off-state. In the turn-off process, the energy loss of the proposed device mainly occurs in Region C due to charging the output capacitance (C_D+C_{FD}), while that of the conventional ones, in Region B due to charging two capacitances of the output capacitance (C_D) and the feedback capacitance (C_{GD}+C_{FD}).



(a) Conventional device (b) Proposed device

Fig. 5. Changes in turn-off characteristics with time at low R_G of 1.07 Ωmm² and a middle R_L of 5.33 Ωmm² with a unit LDMOS layout area of 1 mm². The above characteristics are similar to those obtained under other conditions simulated in this paper.

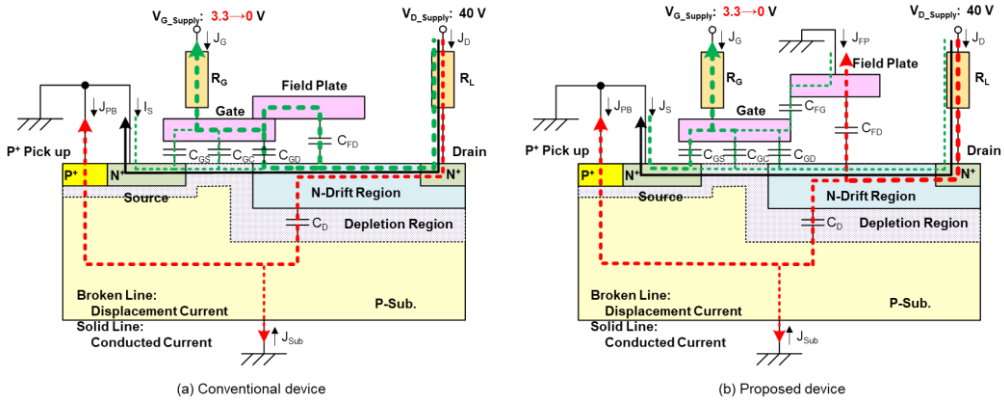


Fig. 6. Current paths in Region B for turn-off process. In Region C of both devices, the conducted current and the current through C_{GC} disappear.

4. Discussion

The proposed device showed unique switching characteristics, the convex-shape gate plateau in the turn-on process and no gate plateau in the turn-off process, caused by the considerably lower feedback capacitance (C_{GD}) despite the higher output capacitance (C_D+C_{FD}). This unique capacitance structure of the proposed device decreases the total energy loss than the conventional one under actual use conditions significantly.

Fig. 7 (a) shows dependences of switching losses of R_L under a low R_G of 1.07 Ωmm^2 (high-speed switching), and Fig. 7 (b), those of R_G under a high R_L of 10.7 Ωmm^2 (light load). Fig. 7 (a) states that the switching loss of the conventional device is much higher than that of the proposed device as R_L decreases (or load becomes heavy). This result is because the switching loss of the conventional device mainly increases in the long gate plateau region as R_L decreases, while that of the proposed device gradually increases as R_L decreases due to the weak Miller effect in a short time. Fig. 7 (b) states that the switching loss of the conventional device is much higher than that of the proposed device as R_G increases. This result is because the gate plateau region for the conventional device affecting the switching loss becomes longer as R_G increases, while the switching loss of the proposed device is almost constant even as R_G increases due to the weak Miller effect.

Fig. 8 shows the switching frequency f dependence of the total energy loss of the proposed device E_{Loss_P} divided by that of the conventional device E_{Loss_C}. The total energy loss consists of the switching loss (turn-on and turn-off) and the conduction loss. Fig. 8 picks up Case A (a low R_G of 1.07 Ωmm^2

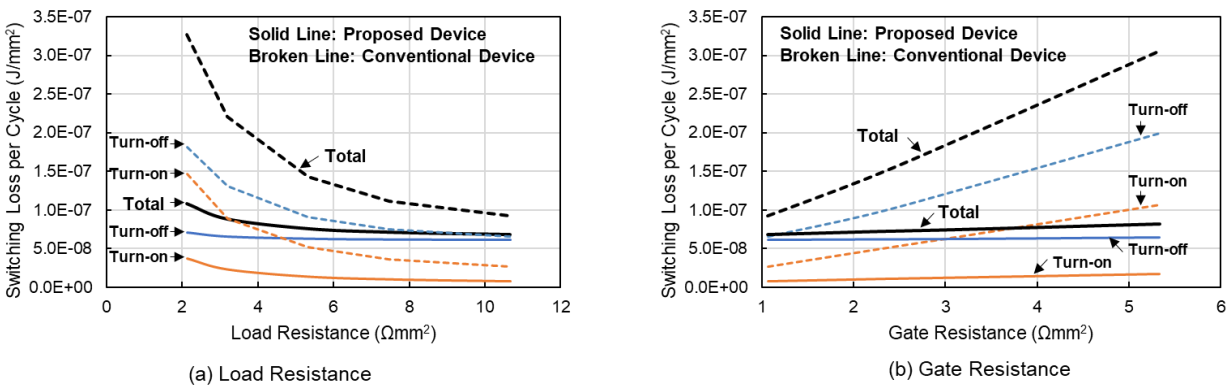


Fig. 7. Dependences of switching losses of (a) R_L under a low R_G of 1.07 Ωmm^2 (high-speed switching) and (b) R_G under a high R_L of 10.7 Ωmm^2 (light load) at a unit LDMOS layout area of 1 mm^2.

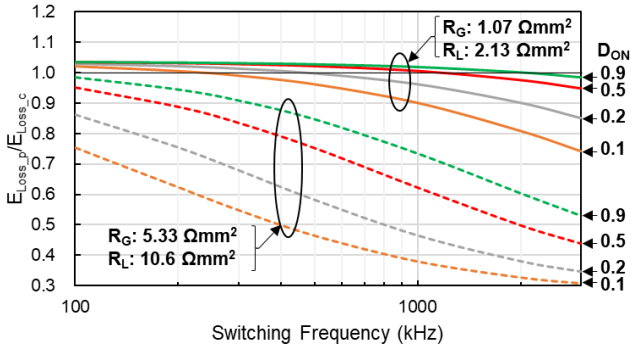


Fig. 8. The switching frequency dependence of the total energy loss ratio E_{Loss_P}/ E_{Loss_C} at a unit LDMOS layout area of 1 mm^2.

and a low R_L of 2.13 Ωmm^2) and Case B (a high R_G of 5.33 Ωmm^2 and a high R_L of 10.6 Ωmm^2) at a device layout area of 1 mm^2. Case A is a good example of containing a high conduction loss, while Case B is a good example of containing a high switching loss. In Case A, although E_{Loss_P}/ E_{Loss_C} decreases with increasing f, E_{Loss_P}/ E_{Loss_C} is higher than one until a high switching frequency range when duty ratio D_{ON} is high. This result is because the specific on-resistance of the proposed device is higher than that of the conventional device. In Case B, E_{Loss_P}/ E_{Loss_C} also decreases with increasing f, and E_{Loss_P}/ E_{Loss_C} attains the lowest value of 0.31 at f = 3 MHz and D_{ON} = 0.1. Therefore, in the actual use condition range, the total energy loss of the proposed device is much lower than that of the conventional device.

5. Conclusion

We have analyzed the switching characteristics of the proposed device in detail by changing R_L and R_G compared with those of the conventional device. The proposed device has a considerably lower feedback capacitance (C_{GD}), although it has a higher output capacitance (C_D+C_{FD}). Under the actual use condition, this unique capacitance structure decreases the switching loss of the proposed device compared with that of the conventional device significantly. The lowest value of E_{Loss_P}/ E_{Loss_C} is 0.31 at f = 3 MHz and D_{ON} = 0.1. The proposed device promises drastically low switching loss under the actual use condition.

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