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Self-biasing Reference Current Source with Two Nagata Current Mirrors Insensitive to Temperature and Supply Voltage

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Abstract. This paper proposes a temperature and supply voltage insensitive CMOS current reference with self-biasing two Nagata current sources. They are fed-back each other and their outputs with appropriate weights are subtracted and then a reference current insensitive to temperature is realized. The proposed circuit is designed in TSMC 180nm process, with 3.3V supply voltage, and our SPICE simulation shows that it achieves a 22μA current and its variation is less than 5% over the temperature range of -20°C to 70°C.

1. Introduction

Current reference is one of the key building blocks in the analog circuit such as amplifiers, oscillators and data converters [1]. At the same time, a reliable reference current independent of process, supply voltage and temperature (PVT) variation is a necessity in the analog IC design. One of the widely used current reference circuits is the peaking current mirror invented by Minoru Nagata in 1966 [1-3], referred to as Nagata current mirror. Several circuit topologies of its modification have been reported [7-10].

In this paper, we consider a reference current source which uses PMOS-type and NMOS-type Nagata current sources fed-back each other with self-biasing configuration for supply voltage insensitivity, and their output current difference with appropriate weights obtained by the subtraction circuit for temperature insensitive characteristics. SPICE simulation results with TSMC 0.18μm CMOS parameters show its verification.

Section 2 provides the analysis of conventional Nagata current mirror, and Section 3 describes the proposed circuit with its simulation result. Then, section 4 provides conclusion.

2. Analysis of Nagata Current Mirror Circuit

The Nagata current mirror has nonlinear input-output current characteristics (Figs. 1, 2); it has a peak with respect to the supply voltage (or the input current) change [1-3]. We derive the mathematical relationship between the input and output currents.

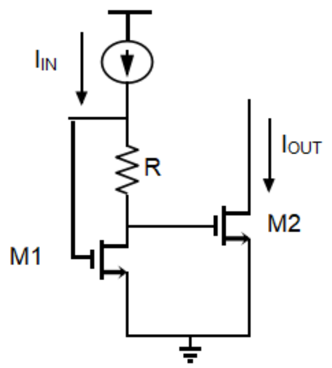

Fig. 1. Nagata current mirror

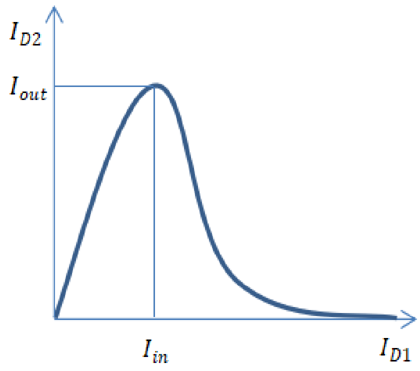

Fig.2. I-O current characteristics of Nagata current mirror

It follows from the Kirchhoff voltage law that

$$V_{GS1} = V_{GS2} + RI_{in} \tag{1}$$

Suppose that the drain currents of M1 and M2 follow the square law in the saturation region, without consideration of the channel length modulation effect for simplicity, we have the following:

$$I_{in} = K_1(V_{GS1} - V_t)^2 \tag{2}$$

$$I_{out} = K_2(V_{GS2} - V_t)^2 \tag{3}$$

Here $K = {}^1\!/_2\, \mu_n C_{ox} \frac{W}{L}$.

Then, the gate-source voltages V_{GS1}, V_{GS2} of M1, M2 can be derived as

$$V_{GS1} = \sqrt{\frac{I_{in}}{K_1}} + V_t \tag{4}$$

$$V_{GS2} = \sqrt{\frac{I_{out}}{K_2}} + V_t \tag{5}$$

Substitute Eq. (4) and Eq. (5) into Eq. (1), and we obtain the output current as

$$I_{out} = K_2R^2(\sqrt{\frac{I_{in}}{K_1R^2}} - I_{in})^2 \tag{6}$$

To find the maximal value of the output current in the Fig.2, we differentiate I_{out} with respect to I_{in}, and we obtain the following:

$$\frac{dI_{out}}{dI_{in}} = 2K_2R^2\left(\sqrt{\frac{I_{in}}{K_1R^2}} - I_{in}\right)\left(\sqrt{\frac{1}{K_1R^2}} \times \sqrt{\frac{1}{4I_{in}}} - 1\right). \tag{7}$$

When $\frac{dI_{out}}{dI_{in}} = 0$, we obtain the following:

$$I_{in1} = \frac{1}{K_1R^2}$$

$$I_{in2} = \frac{1}{4K_1R^2}$$

I_{in2} is the value we need. Substitute it into Eq. (6), and the maxima value of the output current is given as follows:

$$I_{out} = \frac{1}{16K_1R^2} \times \frac{K_2}{K_1}$$

The equation above shows that the output current can be changed by adjusting the resistor values and the MOSFET sizes.

3. Proposed Reference Current Source

3.1 Two Nagata Current Source Circuits Fed-back Each Other with Self-Bias Configuration

As mentioned above, the output current has monotonically increasing property before reaching its peak and reverses after crossing the peak. To achieve a stable output current, the circuit should operate in a negative feedback state. It means that we can make the upper and lower current mirrors have different monotonic properties by adjusting the resistance and MOSFET size appropriately.

As shown in Fig.3 and Fig.4, we adjust the resistor R1 bigger or smaller than R2 to make the circuit operate at point B or A to guarantee a negative feedback state. So the circuit can output a stable current. Here we chose the point B; it means the output current of lower current mirrors has monotonically decreasing properties [4-6]. Actually, because the output current a little bit depends on supply voltage, and the derivative of two current mirrors at point B is different, the input current slightly increases as supply voltage increases. Here, we do not consider the absolute value of the output current, but only focus on its supply voltage dependence.

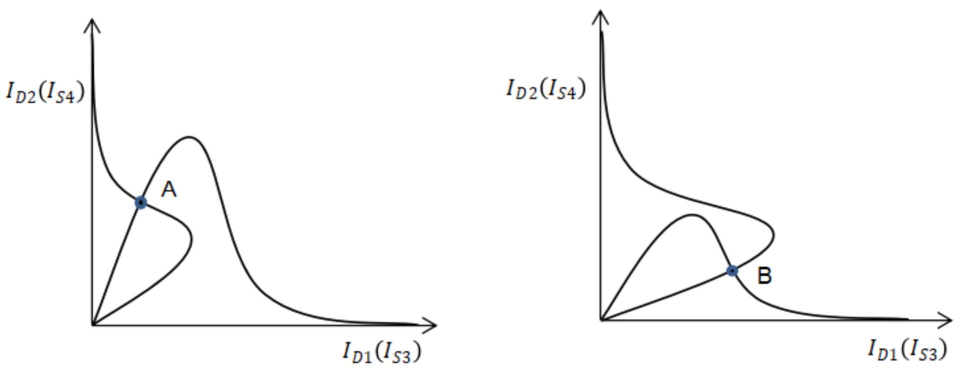

Fig.3. Input-output current characteristics of Nagata current sources.

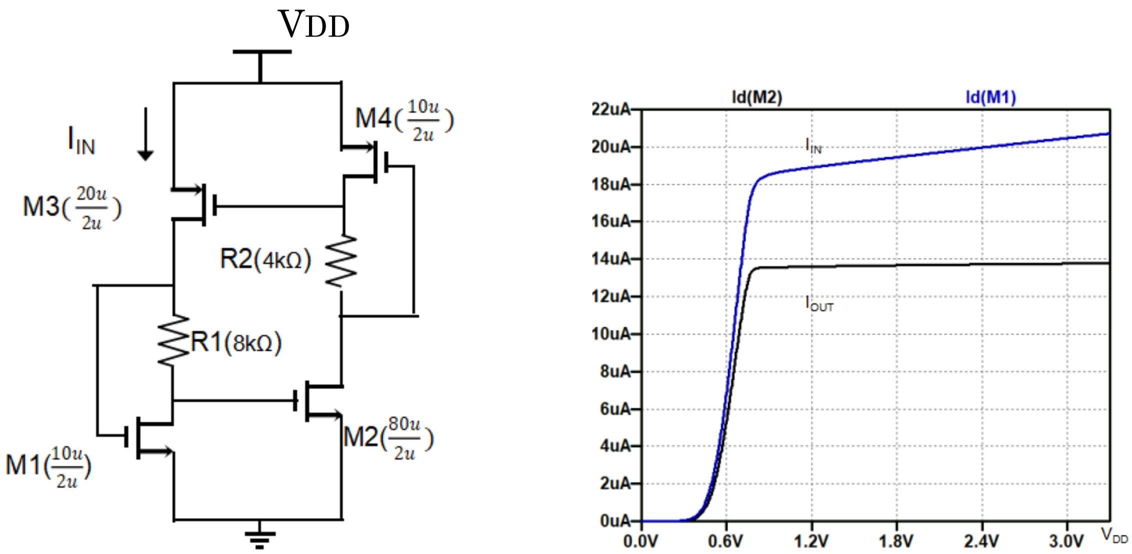

Fig.4. Investigated self-biasing Nagata current mirror circuit and its SPICE simulation result.

3.2 Subtraction Circuit

Although we already have a supply voltage insensitive output current as shown in Fig. 4, it still depends on the temperature (Fig. 5). Since I_{IN} and I_{OUT} both increase when temperature increases, we can make their subtraction for canceling of temperature dependency.

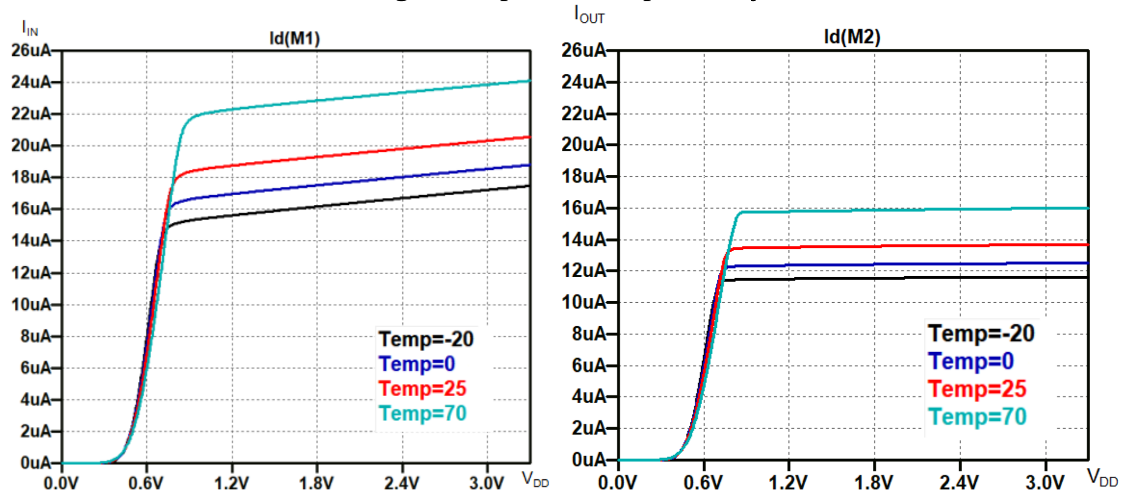

Fig.5. Input and output currents with temperature change.

We see in Fig. 5 that the input current is larger than the output current and slightly depends on the supply voltage, while the output current is insensitive to the supply voltage. So we amplify one output current as I_2 and reduce the other one as I_1 (Fig. 6). The difference current (I_3) between the two currents (I_1, I_2) flows through M7 and it is insensitive to temperature. Then we can re-amplify it by M8 as I_{OUT} to a certain value that we need.

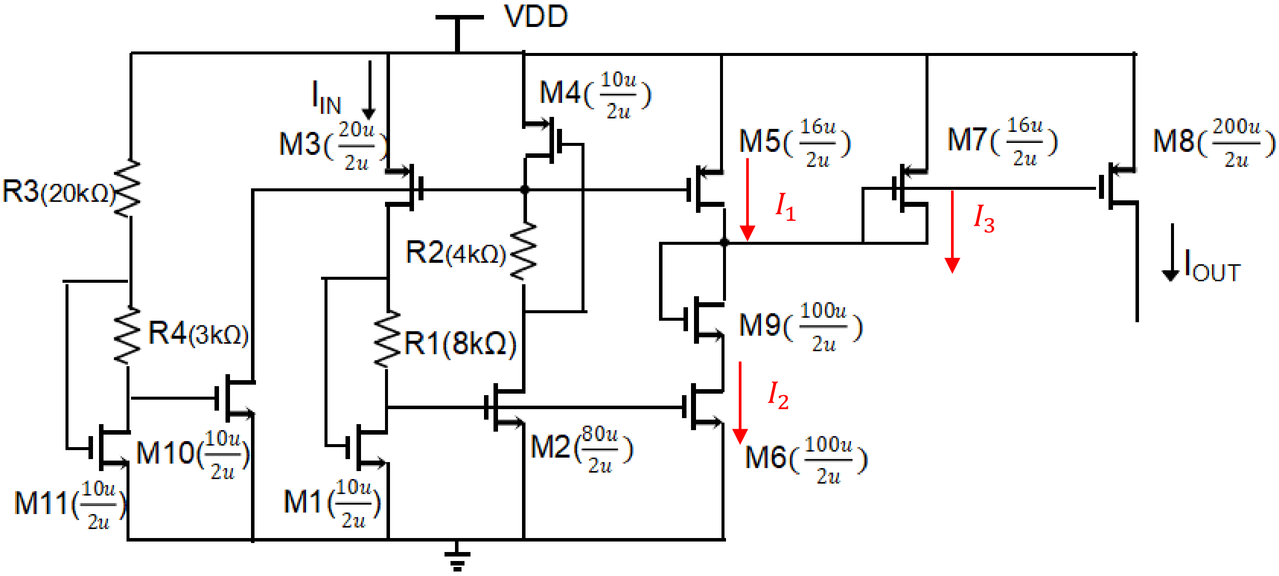

Fig.6. Proposed reference current source with subtraction circuit and start-up circuit.

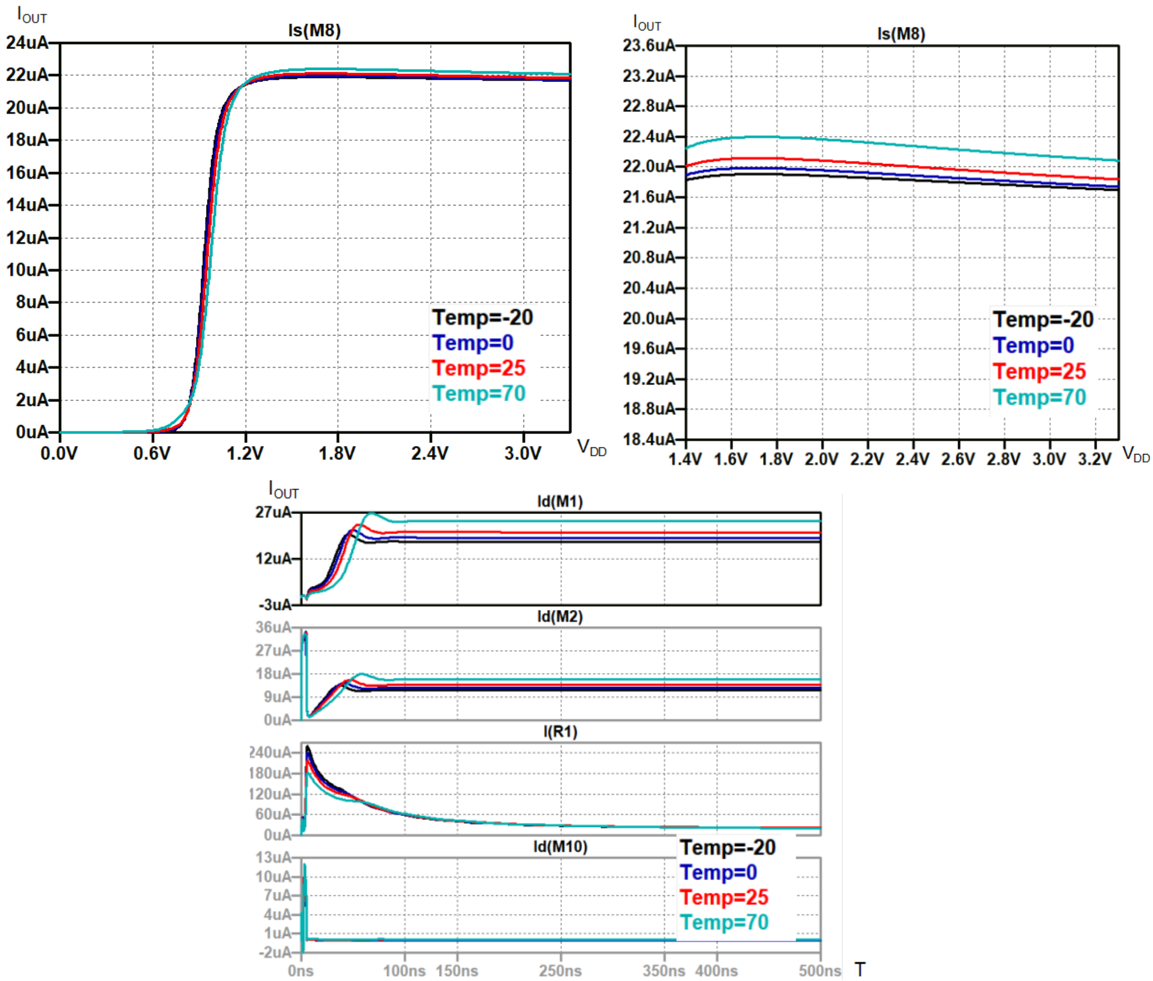

Fig.7. Output current of the reference source circuit in Fig. 6.

When VDD rises, M10 and M11 turns on. The current flowing through M10 and M11 increases that causes the gate potential of M3 decreases. At a certain time, M3 turns on and makes M1, M2 and M4 turn on in order so the whole circuit starts to work. As the current keeps increasing, the gate voltage of M10 becomes lower than its threshold voltage and makes it turn off. We see in Fig. 7 that the circuit operates properly with the start-up circuit when VDD rises from zero to 3.3V in 0.5μs. By adjusting the sizes of MOSFETs in subtraction circuit appropriately, the temperature dependency error can be canceled well; the output current has about 0.8uA error (3.4 % error) over the temperature range of -20℃ to 70℃, and 0.3uA error (1.4 % error) with the supply voltage change between 1.5V to 3.3V.

4. Conclusion

This paper has proposed a CMOS reference current source with two Nagata current mirror circuits fed-back each other. Immunity to the supply voltage is realized using a self-basing configuration and that to the temperature is with the subtraction of the two Nagata current source outputs weighting appropriately. Our SPICE simulation results with TSMC 0.18μm CMOS parameters showed its effectiveness. One of our proposed circuit advantages is that out circuit does not need positive temperature coefficient resistors for realizing the temperature insensitive characteristics.

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