Proceedings of International Conference on Technology and Social Science 2021 (ICTSS 2021)

Comparison of Three Types of Startup Circuits for Self-biasing MOS Reference Current Sources

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Keywords: reference current source, CMOS analog circuit, temperature characteristic, self-biasing circuit, startup circuit

Abstract. This paper studies three startup circuits used in our proposed self-biasing reference current source. First, we present our proposed self-biased MOS reference current source, which is designed with TSMC 0.18μm BSIM3v3 CMOS SPICE parameters, and whose LTspice simulation shows that its output current is insensitive to temperature. Since it has two stable states, a startup circuit is required for its proper operation where finite amount of current flows. Therefore, we consider three types of startup circuits for the proposed circuit, and compare them in terms of chip area, power consumption, and startup operation certainty. We clarify their pros and cons, and show a guideline to select the startup circuit suitable for a specific application of the reference current source circuit.

1. Introduction

In many cases, an analog IC requires a temperature-independent reference current or voltage source [1, 2]. In this paper, we introduce a Gunma University (GU) reference current source [3] as well as its self-biasing function and startup circuit. Its temperature insensitivity of the drain current is realized by setting the gate voltage of the MOSFET to an appropriate value. This circuit has two stable states: one in which some amounts of current flow and the other in which no current flows. So, a starting circuit is required to force some amount of current to flow and settle to the former state [4]. In this paper, three types of startup circuits are studied, and they are compared in terms of chip area, power consumption, and startup operation certainty.

Section 2 shows the NMOSFET drain current (I_{DS}) temperature characteristics, and Section 3 shows the SPICE simulation results of Gunma University (GU) reference current source. Section 4 describes the operation of the three types of its startup circuits and compares their advantages and disadvantages, and Section 5 provides conclusion.

2. Drain Current Temperature Characteristics of MOSFET

In this paper, TSMC 0.18μm BSIM3v3 CMOS SPICE parameters are used in the simulation. Fig. 1 shows the relationship between the gate-source voltage (V_{GS}) and the drain current (I_{DS}) of an NMOSFET. With the gate voltage V_{CP} (cross point gate voltage) the drain current is insensitive to

temperature. At gate voltages higher than V_{CP}, the drain current increases at low temperature, whereas at the gate voltage is lower than V_{CP}, the drain current increases at high temperature [5].

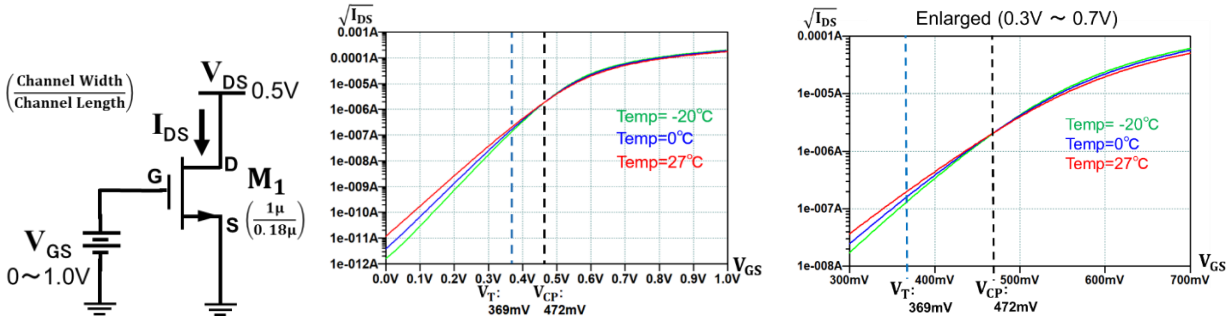

Fig. 1. Drain current temperature characteristics of NMOSFET.

3. Gunma University (GU) Reference Current Source

Fig. 2 shows our proposed MOS reference current source (Gunma University (GU) reference current source). In the stable state, the gate-source voltage of M_{N4} (V_2) is higher than V_{CP}, whereas the gate-source voltages of $M_{N2,5\sim9}$ (V_2-V_4) are lower than V_{CP}. Since I_3 is the sum of M_{N4} and $M_{N2,5\sim9}$ drain currents, the temperature characteristics of the current are cancelled. I_3 is mirrored by the PMOS cascode current mirror (M_{P2}, M_{P5}, M_{P3}, M_{P6}) and I_{OUT} is provided as the output current.

Similarly, I_3 is mirrored by the PMOS cascode current mirror circuit (M_{P2}, M_{P5}, M_{P1}, M_{P4}), and I_1 is injected into the gate voltage generator circuit. However, as I_1 increases, the gate voltage of M_{N4} and M_{N2} increases, and I_3 further increases, which causes a positive feedback effect and makes the circuit unstable. As shown in Fig. 3, when I_1 increases, the gate voltages of M_{N3} and M_{N1} also increase, which makes I_2 increase and I_1 decrease. As a result, the increases of M_{N4} and M_{N2} gate voltages can be suppressed and they settle to stable voltages.

This self-biasing can be achieved by carefully designing the values of R_1 and R_2, and the sizes of M_{N3} and M_{N1}. The gate lengths of M_{N3} and M_{N1} are designed to be large enough so that the drain current is proportional to the square of (V_2-V_T) and ((V_2-V_1)-V_T), respectively, to support self-biasing. The combined drain currents of M_{N3} and M_{N1} also have cancelled temperature characteristics.

Note that since this circuit has two stable states, a startup circuit is needed to operate it in the desired state (current flowing state).

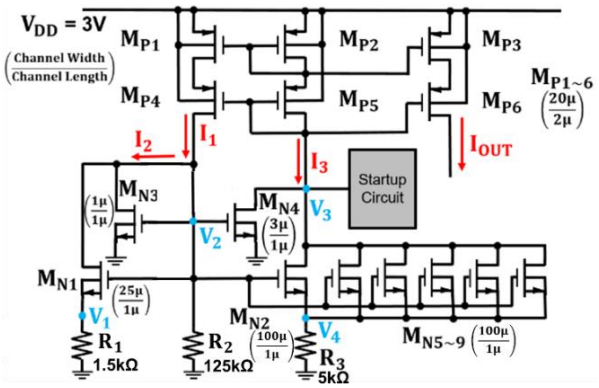

Fig. 2. Self-biasing MOS reference current source.

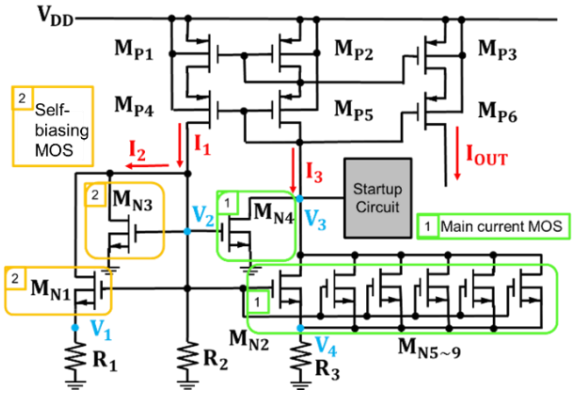

Fig. 3. V_2 suppression by self-biasing MOS.

Fig. 4 shows the output current I_{OUT} of the circuit proposed in Fig. 2. Here, the reference temperature is 27 °C. In the temperature range of -30 °C to + 80 °C, output current fluctuations or relative errors are less than 0.7 [%]. Here, the relative error is defined as the difference between the output current at 27 °C ($I_{OUT(27℃)}$) and the one at p°C ($I_{OUT(p℃)}$) as follows:

$$\text{Error (p℃)} = \left(\frac{I_{OUT(p℃)} - I_{OUT(27℃)}}{I_{OUT(27℃)}}\right) * 100[\%]$$

Fig. 5 shows the gate-source voltages of M_{N2} and M_{N4} in the GU reference current source circuit of Fig. 2. The gate-source voltage of M_{N4} is higher than V_{CP} and that of M_{N2} is lower than V_{CP}.

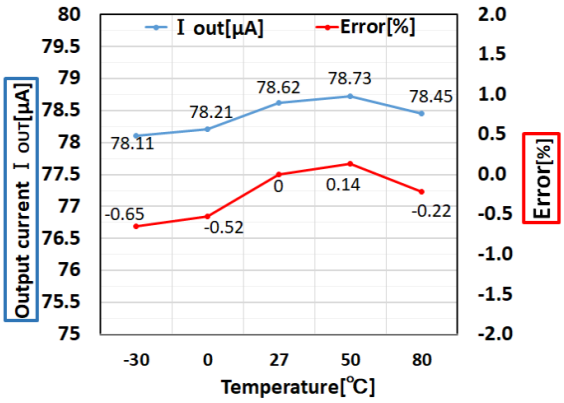

Fig. 4. Output current of the proposed circuit and error from the current at 27 °C.

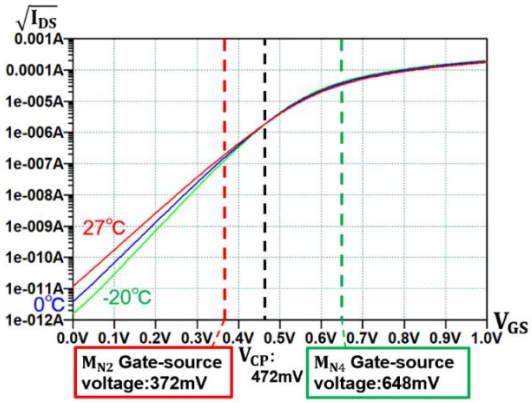

Fig. 5. Gate-source voltages of M_{N2} and M_{N4} (threshold voltage of 369mV).

4. Three Types of Startup Circuit

This section describes operations of three types of startup circuits for the GU reference current source. A self-biasing reference current source circuit has a proper stable operating point A where a desired reference current flows, and a malfunction stable point B where no current flows. Therefore, a startup circuit is used to force the reference circuit to operate at the operating point A.

4.1 Startup Circuit 1

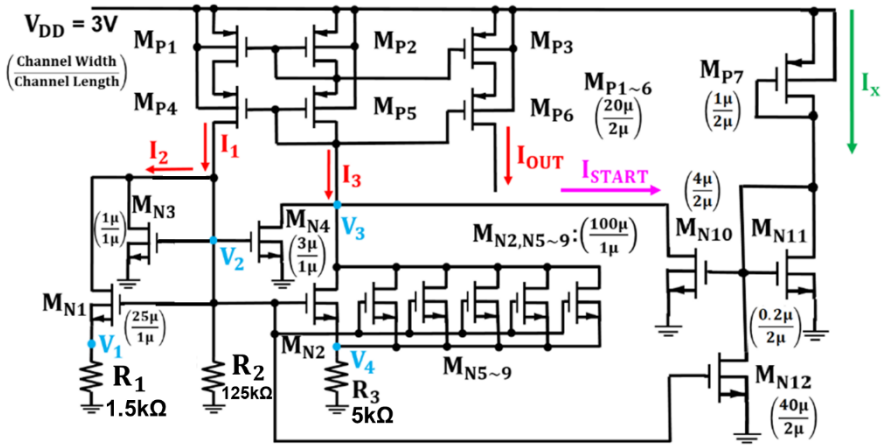

Fig. 6. GU reference current source with startup circuit 1.

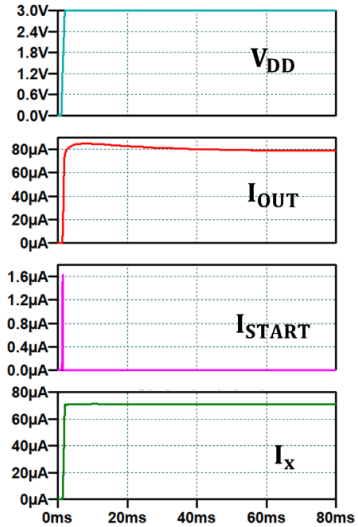

Fig. 7. Simulation result at 27℃.

The startup circuit of Fig. 6 operates as follows:

1) Before the power turns on, all node voltages are 0V. After a while V_{DD} starts to increase, M_{P7} turn on, the gate voltages of M_{N10} and M_{N11} are V_{DD} and M_{N10} turns on.
2) Then the startup current flows through M_{P2}, M_{P5}, and M_{N10} to GND. Due to the PMOS cascode current mirroring, the same amount of the current flows through $M_{P1}$and M_{P4}.
3) The gate voltages of $M_{N2,N5\sim9}$ and M_{N4} increase, and they turn on. Therefore, the current flows along the paths of M_{P2}, M_{P5}, and $M_{N2,N5\sim9}$.
4) As the gate voltage of $M_{N2,N5\sim9}$ increase, the gate voltages of M_{N12} also increases, so that M_{N12} turns on. Eventually, the gate voltage of M_{N10} drops to low voltage and it turns off; the operation as a startup circuit stops.
5) After that, the current continues to flow through M_{P7} and M_{N12} to GND, and M_{N10} keeps off.

We see from Fig. 7 that some amount of current I_X flows through M_{P7} even after the startup operation completes and the normal operation commences. Therefore, there is a problem of non-zero steady current. Then next we introduce the startup circuit 2 for power reduction.

4.2 Startup Circuit 2 (CMOS inverter usage)

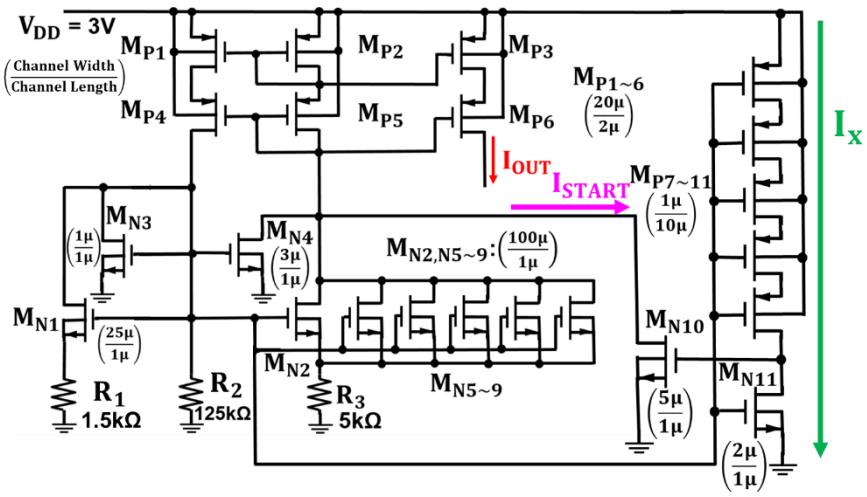

Fig. 8. GU reference current source with startup circuit 2.

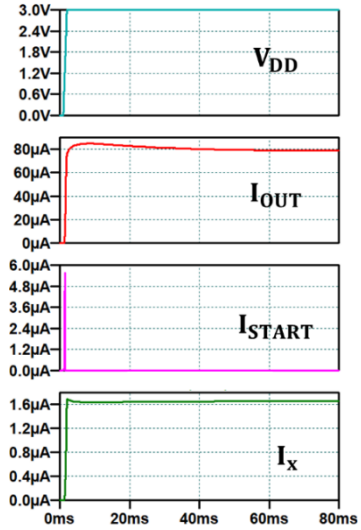

Fig. 9. Simulation result at 27℃.

The startup circuit of Fig. 8 operates as follows:

1) Before the power turns on, all node voltages are 0V. After a while V_{DD} starts to increase, $M_{P7\sim11}$ turn on, the gate voltage of M_{N10} is V_{DD} and M_{N10} turns on.
2) Then the startup current flows through M_{P2}, M_{P5}, and M_{N10} to GND. Due to the PMOS cascode current mirroring, the same amount of current flows through the paths of $M_{P1}$and M_{P4}.
3) The gate voltages of $M_{N2,N5\sim9}$ and M_{N4} increase, and they turn on. Therefore, the current flows along the paths of M_{P2}, M_{P5}, and $M_{N2,N5\sim9}$.
4) As the gate voltages of $M_{N2,N5\sim9}$ increase, the gate voltages of $M_{P7\sim11}$, and M_{N11} also increase, so that $M_{P7\sim11}$ turn off and M_{N11} turns on. Eventually, the gate voltage of M_{N10} drops to GND and it turns off; the operation as a startup circuit stops.

We from Fig. 9 that by suppressing the current I_X, the power consumption could be suppressed as compared with the startup circuit 1. However, the current I_X still flows a little. In addition, it requires a larger number of MOSFETs than the startup circuit 1, which increases the chip area. In the next startup circuit 3, we try to suppress the steady current by using a capacitor.

4.3 Startup Circuit 3 (Capacitor usage)

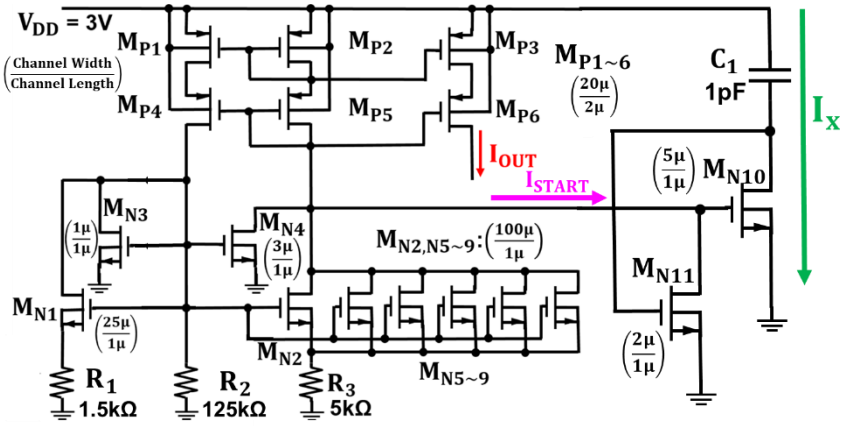

Fig. 10. GU reference current source with startup circuit 3.

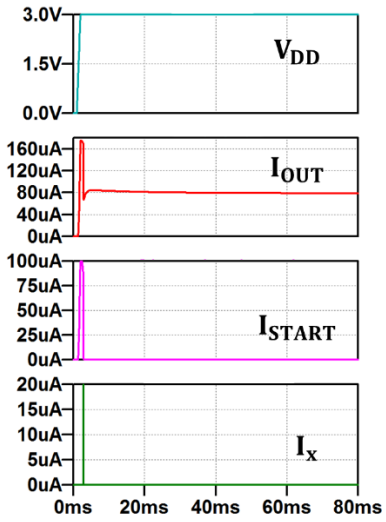

Fig. 11. Simulation result at 27℃.

The startup circuit of Fig. 10 operates as follows:

1) Before the power turns on, all node voltages are 0V. After a while V_{DD} starts to increase, the capacitor C_1 is charged, and the gate voltage of M_{N11} also increases and it turns on.
2) Then the startup current flows through M_{P2}, M_{P5}, and M_{N11} to GND.
3) As the startup current flows, the gate voltage of M_{N10} also increases, so that M_{N10} turns on. As a result, the electric charge in the capacitor C_1 is discharged to GND. Eventually, the gate voltage of M_{N11} drops to GND and it turns off; the operation as a startup circuit stops.

The simulation model of the capacitor is obtained from that of GCH1555C1H1R0CE01 of Murata Manufacturing Co., Ltd. [6]. We see from Fig. 11 that the current I_X became 0 after the circuit started up. Therefore, the power consumption can be reduced compared to the startup circuits 1 and 2.

However, it is pointed out that the startup circuit 3 has a potential risk; when the power supply (V_{DD}) rises very slowly, I_X may be too small to start the proposed circuit. In other words, the startup circuit 3 has a problem in terms of the startup operation certainty. Furthermore, the large value of 1pF is chosen for an on-chip capacitor, and the chip area is larger than that of the startup circuits 1 and 2.

The following table shows a comparison of the three types of startup circuits.

Table. 1. Comparison of three types of startup circuits.

Types of startup circuits	Chip area	Power consumption	Startup certainty
Startup circuit 1	Good	Poor	Good
2 (CMOS inverter usage)	Fair	Fair	Good
3 (Capacitor usage)	Poor	Good	Poor

5. Conclusion

This paper has investigated three types of startup circuits for self-biasing MOS reference current sources insensitive to supply temperature and voltage (Gunma University (GU) reference current source) and simulated each circuit. We have compared them in terms of chip area, power consumption, and startup certainty. As a result, we found that each of them has its own advantages and disadvantages, and it is necessary to select the optimal startup circuit according to the application of the proposed circuit.

Comparison of the similar CMOS reference current sources [10, 11] is next work.

Acknowledgements

This work is supported by Adaptable and Seamless Technology Transfer Program through Target-Driven R&D (A-STEP) from Japan Science and Technology Agency (JST) Grant Number JPMJTR201C.

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