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Generalized Leslie-Singh Architecture of 1st order Delta-Sigma AD Modulator with Different Resolutions of ADC and DAC

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Abstract. This paper presents generalized Leslie-Singh architecture of 1st order ΔΣAD modulator using multi-bit ADC and DAC. The original Leslie-Singh architecture ΔΣ AD modulator uses a multi-bit ADC and a single-bit DAC inside the modulator. Here we consider an *m*-bit ADC and an *n*-bit DAC with $m \geq n \geq 1$, inside the modulator. SQNDR of the modulator with various (m,n) is investigated by simulations and it is found that as *m* increases by 1, SQNDR improves by 6dB, while as *n* increases by 1, SQNDR improves by 3dB for $m \gg n$ but it saturates for $m \approx n$.

1. Introduction

A multi-bit ΔΣ AD modulator receives much attention because the quantization noise of the ADC inside is reduced. The multi-bit ADC inside the modulator improves the signal-to-[quantization noise + distortion] ratio (SQNDR) by 6 dB for 1-bit resolution increase [1]. In many cases, a 3-bit flash is used as a multi-bit ADC because more than 3-bit flash ADC requires large hardware and power. Also, the multi-bit DAC improves the high-order modulator loop stability as well as the integrator operational amplifier swing inside the modulator is reduced, which is suitable for low power. For a continuous-time modulator, the multi-bit DAC clock jitter effects are alleviated. However, the multi-bit DAC nonlinearity causes overall ΔΣ ADC nonlinearity and hence some care such as employment of data-weighted-averaging (DWA) logic is needed [1].

Then the Leslie-Singh or Yoshitome-Uchiyama Δ Σ AD modulator architecture was proposed in [2, 3], where a multi-bit ADC and a single-bit DAC are used inside the modulator. It keeps the advantage of quantization noise reduction while the DAC nonlinearity problem is avoided because the single-bit DAC is inherently linear. However, it loses the multi-bit DAC advantages of higher-order loop stability and the operational amplifier swing reduction.

We proposed a charge-domain CMOS folding ADC which is fast comparable to the flash-type and it requires only *m* comparators for *m*-bit resolution [4]. A 5-bit or 6-bit charge domain CMOS folding ADC can be used inside the ΔΣ AD modulator in practice, thanks to its low power and small hardware.

Then we consider the generalization of the Leslie-Singh ΔΣ AD modulator architecture where an *m*-bit ADC and an *n*-bit DAC with $m \geq n \geq 1$ are used. *m* can be as large as 6 and in such a case, *n* is not necessarily equal to *m* for hardware and power reduction; in other words, if a flash-type ADC is employed inside the modulator, its resolution is limited up-to 3 or 4-bit due to the power and hardware restriction, but when the charge domain folding ADC is used, its resolution is extended up-to 5 or 6-bit, which motivates the present study. As the first step, we have investigated the 1st order modulator case using simulation.

In this paper, Section 1 describes the introduction of multi-bit ΔΣ AD modulator. Section 2 presents the Leslie-Singh architecture of the 1st order ΔΣ AD modulator, and Section 3 shows its simulation results. Finally, Section 4 provides the conclusion.

2. Generalized Leslie-Singh Architecture of 1st order ΔΣ AD Modulator

Leslie and Singh proposed a ΔΣAD modulator which uses a multi-bit ADC and a single bit DAC. It can reduce the quantization noise of the ADC inside the modulator and avoid nonlinearity of the DAC; this is because the single-bit DAC is inherently linear whereas the multi-bit DAC has some nonlinearities. We have mentioned a ΔΣAD modulator which uses a 6-bit or 5-bit folding ADC and a 3-bit DAC with the data-weight-averaging (DWA) algorithm logic, as the extension of the Leslie-Singh architecture and as well as an application of the charge domain folding ADC [4].

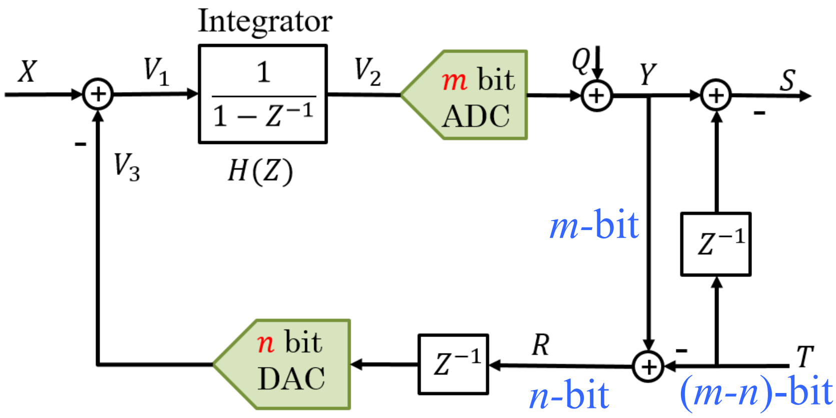


Fig. 1. Generalized Leslie-Singh architecture of 1st order ΔΣAD modulator.

We investigate here our generalized Leslie-Singh architecture of 1st order ΔΣAD modulator (Fig.1). It is composed of an analog integrator, a comparator (m-bit ADC) and an n-bit DAC ($m \geq n \geq 1$). The modulator output is expressed as follow:

$$Y(Z) = V_2(Z) + Q(Z)$$
$$= \frac{1}{(1 - Z^{-1})}\{X(Z) - Z^{-1}[Y(Z) - T(Z)]\} + Q(Z)$$
$$= X(Z) + Z^{-1}\ T(Z) + (1 - Z^{-1})Q(Z) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots. (1)$$

Here, $X(Z)$ is the input signal, $Y(Z)$ is the m-bit ADC output, $Q(Z)$ is the ADC quantization noise, $S(Z)$ is the modulator output, $H(Z)$ is the analog integrator transfer function and $T(Z)$ is the lower $(m - n)$ bits of n-bit DAC. Here, the DAC input *R(Z)* is the upper *n* bits of *Y (Z)* and the truncation signal $T(Z)$ is expressed as the following:

$$T(Z) = Y(Z) - R(Z) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots. (2)$$

Then, the final output of the modulator *S(Z)* can be expressed as:

$$S(Z) = Y(Z) - Z^{-1}T(Z) \quad \ldots\ldots (3)$$

Substituting Eq. (1) into Eq. (3), the modulator output *S(Z)* can be written as:

$$S(Z) = X(Z) + (1 - Z^{-1})Q(Z) \quad \ldots\ldots (4)$$

Here, we see that the signal transfer function is 1 ($STF(Z) = 1$), while the noise transfer function shows that the quantization noise is the first-order noise shaped ($NTF(Z) = 1 - Z^{-1}$).

3. Simulation Results

The generalized Leslie-Singh architecture of 1st order ΔΣAD modulator in Fig.1 is simulated using MATLAB with simulation parameters in Table 1.

Table1. Simulation parameters

ADC *m* [bit]	DAC *n* [bit]	Input Signal	Amplitude @max value	Input freq. Sampling freq.	Data points
1	1	Sine wave	0.9	$1/2^{20}$	2^{20}
2	1		1.9		
2	2		2.9		
3	1		3.9		
3	2		5.9		
3	3		6.9		
4	1		7.9		
4	2		11.9		
4	3		13.9		
4	4		14.8		
5	1		15.9		
5	2		23.7		
5	3		27.8		
5	4		29.7		
6	1		31.9		
6	2		47.5		
6	3		55.7		
6	4		59.6		
6	5		61.9		

The simulation results of the over sampling ratio (OSR) versus SQNDR for the modulator with a multi-bit ADC and a single-bit DAC are shown in Fig. 2. Here, OSR and SQNDR are evaluated by the following equations:

$$OSR = \frac{f_s}{2 \cdot B} \quad \ldots\ldots (5)$$

$$SQNDR = 10\,log(\frac{Signal\ \ power}{\Sigma(Noise + distortion)\ \ power}) \quad \ldots\ldots (6)$$

The simulation results show that a multi-bit ADC improves the linearity and the quantization noise is reduced. We see in Fig 2 that a 6-bit ADC inside the modulator has the best linearity and the corresponding AD modulator achieves the high SQNDR.

Fig. 3 shows the results of SQNDR at $\mathrm{OSR} = 2^5$ of the original Leslie-Singh 1st order $\Delta\Sigma$ AD modulator with a multi-bit ADC and a single-bit DAC. We discovered that for 1-bit to 2-bit ADC the SQNDR increases by 3 [dB], whereas for 2-bit ADC to 6-bit ADC, SQNDR increase by 6 [dB] for every ADC resolution increase by 1-bit. This result is supported by the following equation:

$$SQNDR = 6.02m + 1.76 \ \ [dB] \tag{7}$$

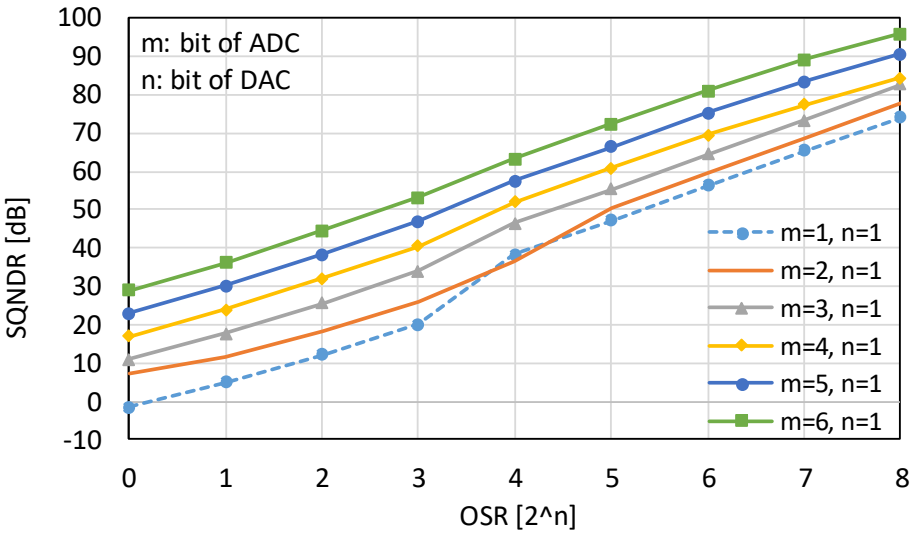


Fig. 2. OSR versus SQNDR of the 1st-order Leslie-Singh modulator with various resolutions of the multi-bit ADC.

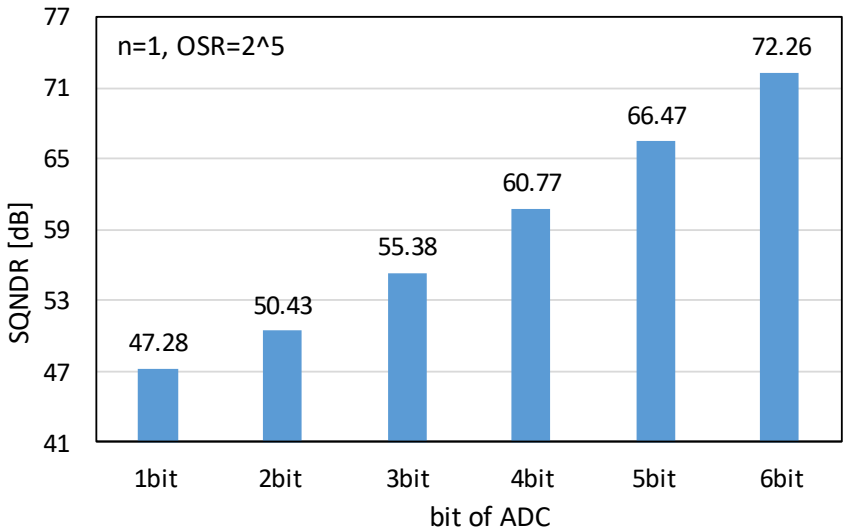
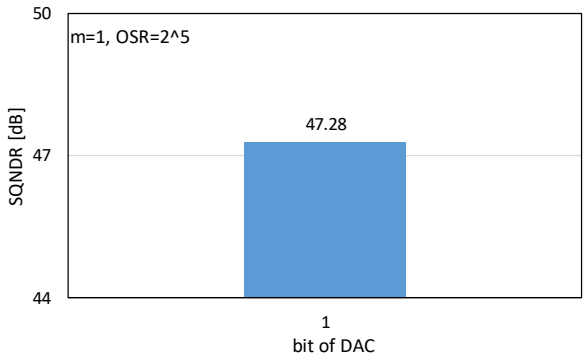
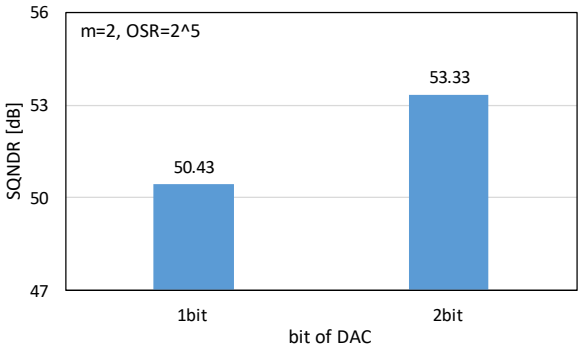


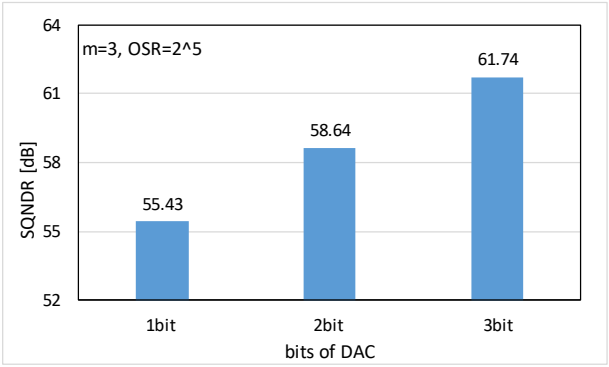
Fig. 3. SQNDR versus multi-bit ADC resolution at $\mathrm{OSR} = 2^5$ of the 1st order Leslie-Singh modulator.



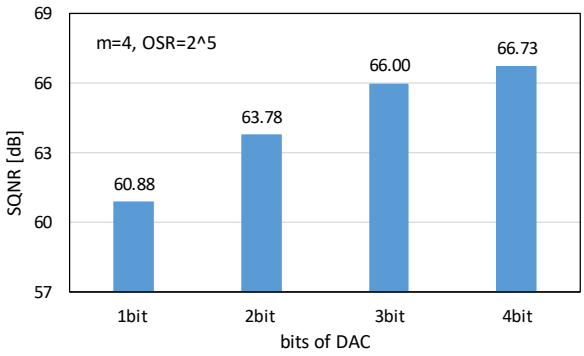
(a) 1-bit ADC



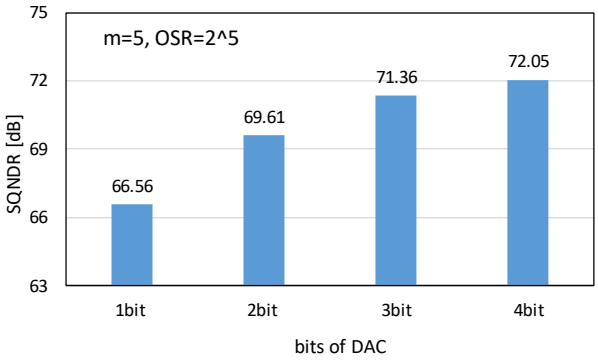
(b) 2-bit ADC



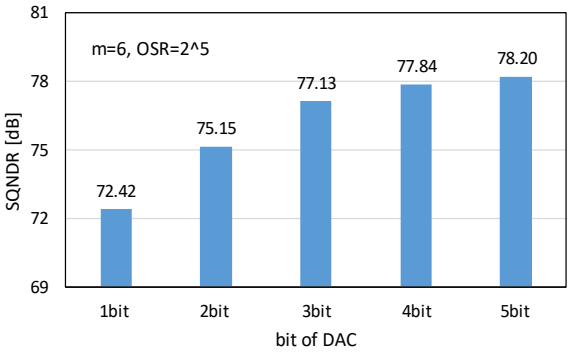
(c) 3-bit ADC



(d) 4-bit ADC



(e) 5-bit ADC



(f) 6-bit ADC

Fig. 4. SQNDR at $\mathrm{OSR} = 2^5$ in case of multi-bit ADC and DAC usage inside the modulator.

The simulation results of SQNDR at $\mathrm{OSR} = 2^5$ which uses a multi-bit DAC are shown in Fig. 4. The results in Fig. 4 (f) show that from 1-bit DAC to 3-bit DAC, as every 1 bit increases, SQNDR is increased by 3 [dB]. However, more than 3-bit DAC may lead to large hardware and power with only small SQNDR improvement, and the 3-bit DAC may suffice in 6-bit ADC usage case. The summarized simulation results of SQNDR at $\mathrm{OSR} = 2^5$ which uses (m, n) bits inside the modulator are shown in Table2.

4. Conclusion

The generalized Leslie-Singh architecture of 1st order ΔΣAD modulator using multi-bit DAC have been investigated. SQNDR of the multi-bit ΔΣAD modulator is analyzed and compared for various combinations of the ADC and DAC resolutions. The simulation results show that for 1-bit resolution increase of the multi-bit ADC, SQNDR is increased by 6 dB whereas for 1-bit resolution increase of the multi-bit DAC, SQNDR is increased by 3 dB. A multi-bit DAC improves the modulator loop stability and the reason why the DAC resolution increase leads to SQNDR improvement would be the maximum input amplitude increase with keeping stability.

As the next step, we will investigate the generalized Leslie Singh architecture of the 2nd-order AD modulator.

Table2. Summarized of the simulation results

ADC *m* [bit]	DAC *n* [bit]	Input Signal	Amplitude @max value	Input freq. Sampling freq.	Data points	SQNDR [dB] @OSR = 2^5
1	1	Sine wave	0.9	$1/2^{20}$	2^{20}	47.29
2	1		1.9			50.40
2	2		2.9			53.30
3	1		3.9			55.40
3	2		5.9			59.03
3	3		6.9			61.30
4	1		7.9			60.50
4	2		11.9			63.45
4	3		13.9			65.75
4	4		14.8			67.45
5	1		15.9			66.47
5	2		23.7			69.33
5	3		27.8			71.48
5	4		29.7			72.17
6	1		31.9			72.26
6	2		47.5			75.15
6	3		55.7			76.97
6	4		59.6			77.84
6	5		61.9			78.20

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