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Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorting with Digital Method

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Abstract. This paper describes a self-calibration method for a current-steering Digital-to-Analog Converter (DAC) with a voltage-controlled oscillator (VCO). It is a digital method and does not require high precision analog circuits; the VCO needs only monotonic characteristics but it does not need linearity. Mismatches among the unit current sources in the current-steering segmented DAC cause the overall DAC nonlinearity, and the VCO measures the order of each current source value. The measured information is stored in memory, and based on it, each current source is sorted to reduce the DAC nonlinearity. Especially we have investigated with simulations whether the sorting algorithms can improve the DAC Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) with several mismatch conditions. We present its principle and simulation results.

1. Introduction

Digital-to-Analog Converter (DAC) is a key component for modern transmitter circuits, and there its high linearity is required. For its nano-CMOS implementation, the device mismatch is large and hence the analog circuit characteristics may be deteriorated. However, there, digital circuit can be implemented with small chip area and hence so-called the digitally-assisted analog technology is attractive.

This paper investigates the DAC linearity improvement algorithm and circuit; the DAC under investigation employs the current-steering segmented architecture for high-speed and low glitch applications as shown in Fig. 1.

We mainly examine the switching sequence post adjustment (SSPA) algorithm [1] using simulation in details, and its digital-oriented implementation without an analog current comparator. We have found that the SSPA algorithm can be more effective in large mismatch cases. Notice that here the sorting algorithm is based on the unit current cell value measurement results. However, in another research in [2], the measurement is not performed but the sorting is based on the systematic error tendency depending on the unit cell layout position. In comparison, the SSPA method is expected to accurately estimate the reducing ratio of DNL and INL.

2. Problem Formulation

Consider the segmented current-steering DAC in Fig. 1. Ideally the designed current sources satisfy the following:

$$I_1 = I_2 = I_3 = \ldots = I_N. \quad (1)$$

However, in reality, due to device mismatches, they are not identical and expressed as follows:

$$I_1 = I + \Delta I_1,\ I_2 = I + \Delta I_2,\ I_3 = I + \Delta I_3,\ldots,\ I_N = I + \Delta I_N. \quad (2)$$

Here I is defined as their average of I_1, I_2 , I_3 ,…and I_N:

$$I = \frac{1}{N}\,[I_1 + I_2 + I_3 + \ldots + I_N]. \quad (3)$$

ΔI_1, ΔI_2, ΔI_3,…, and ΔI_N can be positive, zero or negative. The sum of the mismatches can be obtained from Eqs. (2) and (3) as follows:

$$\Delta I_1 + \Delta I_2 + \Delta I_3 + \ldots + \Delta I_N = 0. \quad (4)$$

The DAC operation in Fig. 1 is as follows: For the DAC input of zero, all switches are off, and the analog output of $V_{OUT} = 0$. For the DAC input of one, the switch of S_1 is on and $V_{OUT} = R\ I_1 = R\ (I + \Delta I_1)$. For the DAC input of two, S_1 and S_2 are on and $V_{OUT} = R\ (I_1 + I_2) = R\ (2\ I + \Delta I_1 + \Delta I_2)$. Similarly, for the DAC input of k, $V_{OUT} = R\ (I_1 + I_2 + \ldots + I_k) = R\ (\mathrm{k}\ I + \Delta I_1 + \Delta I_2 + \ldots + \Delta I_k)$.

We see that non-zero values of ΔI_1, ΔI_2, ΔI_3,…, and ΔI_N can cause the DAC nonlinearity. Let us consider to select n1-th, n2-th,.. and nk-th, current sources for DAC input of k, as follows:

$$V_{OUT} = R\ (I_{n1} + I_{n2} + \ldots + I_{nk}) = R\ (\mathrm{k}\ I + \Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}) \quad (5)$$

If the following is satisfied

$$|\Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}| < |\Delta I_1 + \Delta I_2 + \ldots + \Delta I_k| \quad (6)$$

then the integral nonlinearity at the input k can be reduced. In this paper, we investigate the unit cell selection algorithm which minimizes $|\Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}|$ as much as possible.

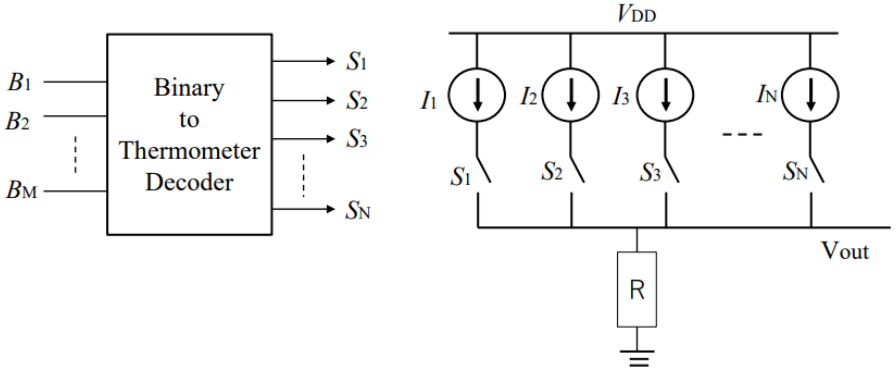


Fig. 1. Segmented current-steering DAC configuration.

3. Unit Current Cell Sorting Algorithm

We investigate here unit current cell sorting techniques. Notice that we can measure the order from the smallest to the largest unit current cell values with a digital method; we measure the number of the VCO cycles during long enough constant time by a digital counter, as explained in the next section.

Now we explain the switching sequence post adjustment (SSPA) algorithm [1] for delay cell sorting. The SSPA is a calibration method that can change the switching sequence of delay cells especially after fabrication process, and a very good integral linearity of the DAC can be obtained. Its algorithm is as follows (Fig. 2):

1) The values of the unit current cells are measured with the VCO though it is not linear, but monotonicity is kept, and they are sorted in the memory from the lowest to the highest order.
2) Then, the sorted unit current cells are rearranged by arranging small unit current cells between two large cells, using the CPU.
3) After that, each two neighboring unit current cells are summed.
4) Then summed unit current cells are again measured and sorted as 1).
5) They are rearranged as 2).
6) Finally, the final sequence is obtained.

Remark:
(i) Current summation can be done simply with their connection in parallel, obeying the Kirchhoff current law.
(ii) We can have redundant unit current cells. For example, we have N+2 unit current cells and discard two cells with the largest and the smallest unit current cells, and we perform the same method to the remaining N unit current cells as described above.

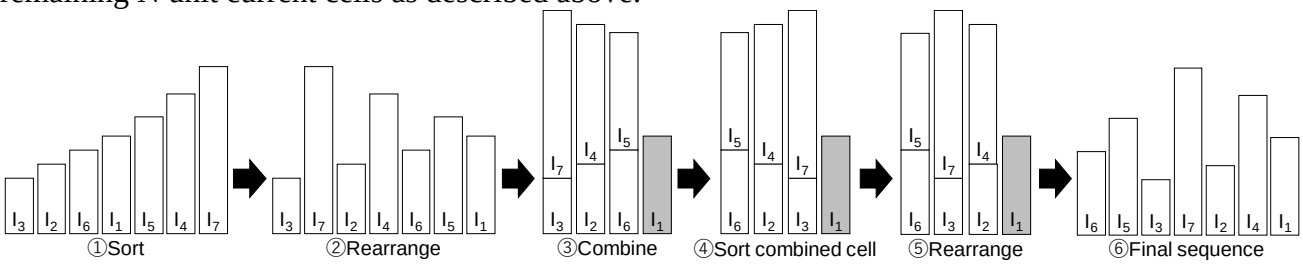


Fig. 2. Explanation of the switching sequence post adjustment algorithm.

4. Simulation Results

Assuming a 7-bit DAC, 127 current sources are used in this simulation. The current sources have mismatches as shown in Eq. (2). In this study, the current source was assumed to vary in a normal distribution with standard deviation σ (defined as SD/2) around the mean value *I* defined by Eq. (3). It means that it varies within the range of SD [%] concerning the magnitude *I* of the current source. An example for I=1.0 and SD=5, 10, and 20 are shown in Fig. 3. The larger the SD, the larger the mismatches. The simulation was performed by varying the degree of mismatches from 1% to 20% as parameter SD. The mismatches are calculated using the standard rand function of C language, using the current time as the seed of the rand function. Since each run produced a different value, we ran the simulation 10 times. For each simulation, INLpp and DNLpp were calculated according to Eqs (7) and (8). In other words, we obtained INLpp and DNLpp for 10 times. 10 INLpp and DNLpp were arithmetically averaged, respectively. The difference between the maximum and minimum values of INL of 127 current sources is defined as INLpp as follows:

$$INLpp=maximum(INL_{k1})-minimum(INL_{k2}) \quad (7)$$

In the same way, DNLpp is as follows:

$$DNLpp=maximum(DNL_{k3})-minimum(DNL_{k4}) \quad (8)$$

The values of INLpp and DNLpp before and after SSPA are analyzed. The average values of the data obtained from 10 times of simulation are shown in Figs. 4 and 5. And the maximum and minimum values are shown in Figs. 6 and 7, respectively.

Fig. 4(a) shows the DNLpp before and after SSPA. Fig. 5(a) shows the INLpp before and after SSPA. The DNLpp and INLpp tended to increase as the SD increased. The percentages of DNLpp and INLpp before SSPA are shown in Figs. 4(b) and 5(b). DNLpp and INLpp were reduced by about 40% and 60%, respectively, by SSPA. These percentages are almost the same for all SDs. That is to say, the larger the SD is, the larger the absolute value of DNLpp and INLpp reduction is. After SSPA, DNLpp increases in proportion to SD (DNLpp = 0.025 × SD).

The maximum and minimum values of DNLpp from 10 simulations are shown in Fig. 6. The SSPA is greatly reduced the maximum value of DNLpp as shown in Fig. 6 (a). As a result, the average value of DNLpp is also reduced as shown in Fig. 4. INLpp is shown in Fig. 7 as well. SSPA is significantly reduced the minimum value of INLpp. It reduced the average value of INLpp, as shown in Fig. 5.

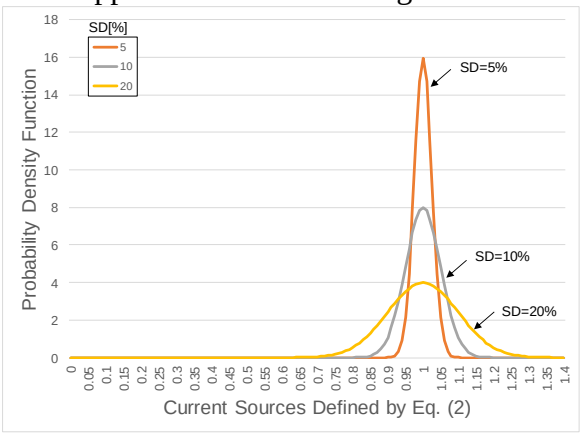
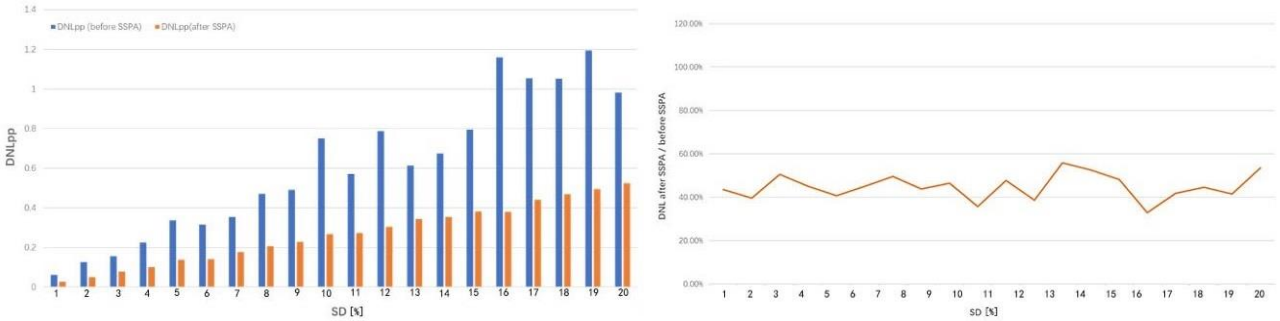
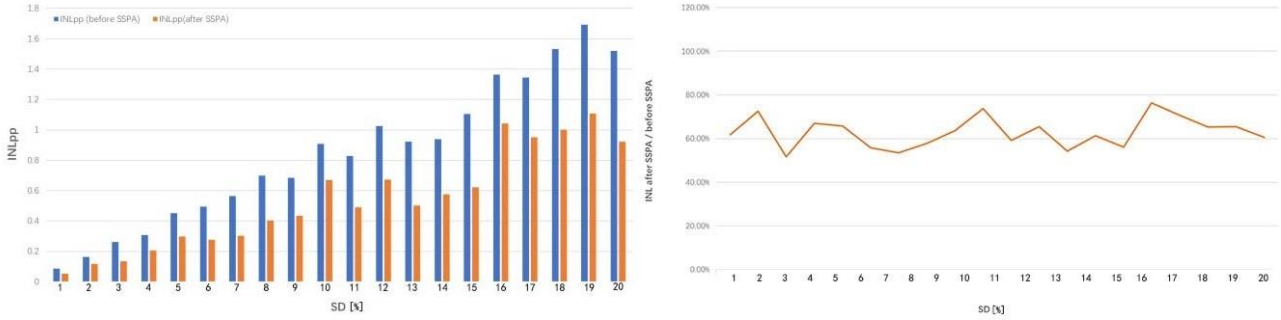


Fig. 3. Example of the current sources mismatches.



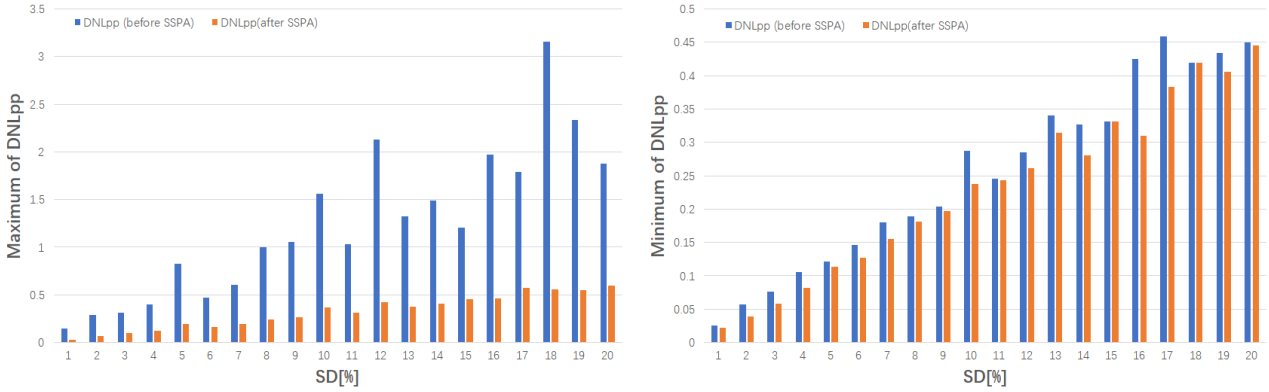
(a) DNLpp before SSPA and after SSPA (b) Reduction ratio by SSPA

Fig. 4. DNL reduction with SSPA



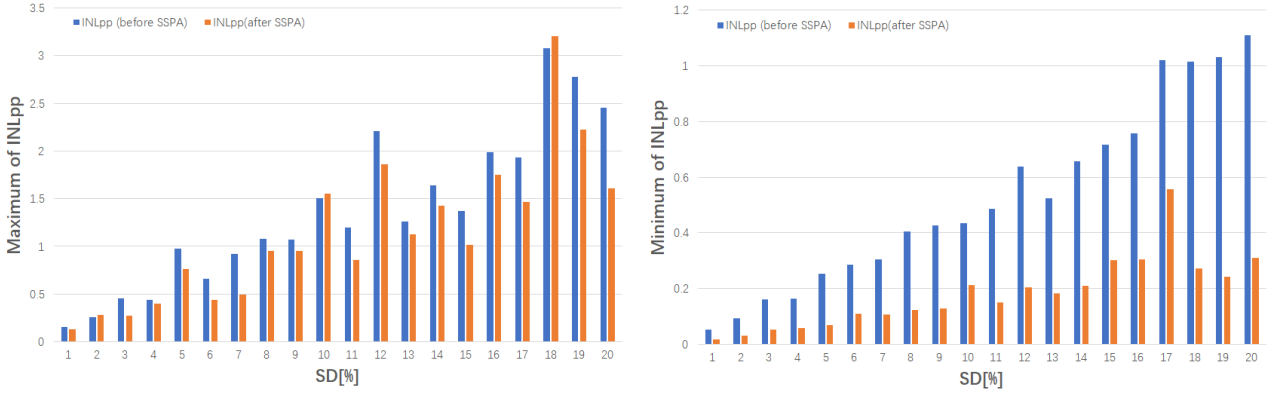
(a) INLpp before SSPA and after SSPA (b) Reduction ratio by SSPA

Fig. 5. INL reduction with SSPA



(a) Maximum value (b) Minimum value

Fig. 6. Maximum and minimum value of DNLpp during 10 times of simulation.



(a) Maximum value (b) Minimum value

Fig. 7. Maximum and minimum value of INLpp during 10 times of simulation.

5. DAC Architecture with Sorting Algorithm

Fig. 8 shows the segmented current-steering DAC with the sorting algorithm.

During calibration mode:

The CPU controls the switches one by one, and the VCO and the binary counter measure each unit current cell value as a digital value and stored in the memory. Then the CPU performs the above-mentioned sorting algorithm: two switches are on and again the VCO and the binary counter measure the sum of them. Their measured values and their order information are stored in the memory.

During normal mode:

The binary input data are decoded into the thermometer code data, and combined with the calibration data stored in the memory, the switches are controlled.

Fig. 9 shows a VCO circuit with current-controlled inverters and START circuit.

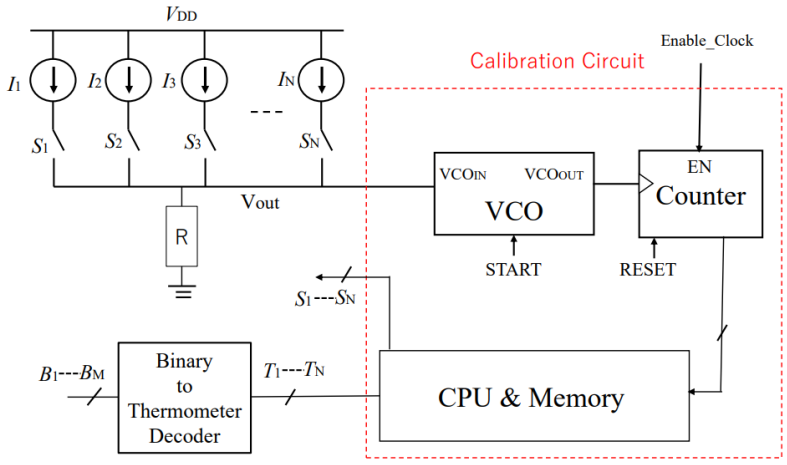


Fig. 8. Explanation of the switching sequence post adjustment algorithm.

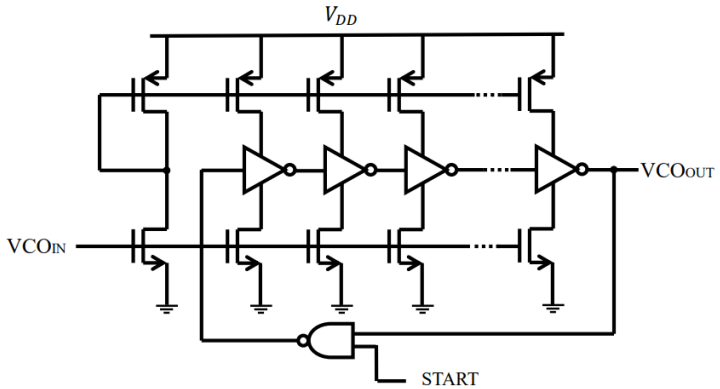


Fig. 9. VCO circuit with current-controlled inverters and START circuit.

6. Conclusion

This paper has investigated the segmented current-steering DAC linearity improvement algorithm using the unit current cell sorting. Our simulation results show that SSPA can reduce DNL by about 40% and INL by about 60%. Therefore, the larger the mismatches of the current source, the larger absolute values of DNL and INL can be reduced. We also consider the unit current cell method in a digital manner. These techniques are suitable to digital-oriented advanced CMOS circuit implementation.

Acknowledgements

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