Proceedings of International Conference on
Technology and Social Science 2021 (ICTSS 2021)

Revival of Asynchronous SAR ADC based on Hopfield Network

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Keywords: SAR ADC, Asynchronous, Non-binary, Hopfield Network, Resistive Network

Abstract. This paper describes an asynchronous successive-approximation-register (SAR) ADC based on the Hopfield network, which consists of a resistive network and inverters. It can avoid local minima due to the discard of the feedback paths, and it does not need an SAR logic circuit. Its design is very simple and it can operate very fast. Also by proper design of resister values, a non-binary weight SAR ADC can be realized for high reliability, besides a binary weight SAR ADC.

1. Introduction

The Hopfield network has been investigated as an ADC architecture for several tens of years [1], but it has not been widely used in practice. Here we revisit the Hopfield network and consider several interesting configurations. We expect that resistive networks such as the Hopfield network and the active resistive network [2] besides resistive DACs [3, 4] revive in analog signal processing fields.

It is known that the Hopfield network ADC often falls into the so-called local minimum, which means high error rate and which makes it impractical for commercial application. However, the Hopfield network ADC is attractive because it is very fast, its operation is asynchronous and its design is simple. We consider that its modification may lead to a high performance reliable asynchronous SAR ADC, which is now a very hot topic in ADC research fields, and hence we revisit the Hopfield network ADC here. We have improved the Hopfield network ADC by discarding the feedback paths from the lower bits to the upper bits to avoid the local minima problem. We also show that a non-binary weighted SAR ADC can be realized by proper design of resistor values; as an example, we show a Fibonacci number weighted SAR ADC. Further we point out that the improved Hopfield network ADC has a DAC array inside the network. These are verified with SPICE simulations.

2. Traditional Hopfield Neural Network ADC

It is well-known that the ADC based on the traditional Hopfield neural network (Fig.1) [1] has a problem of local minima (Fig.2), which sometimes leads to wrong output. Its reason is that there are feedback pats from lower bits to higher bits. Fig. 2 explains the local minima problem. Consider the case to obtain the parameter where the potential energy is at minimum using the gradient calculation of the potential energy. Sometimes, the potential energy gradient calculation may fall into the local minima; in such a case, it cannot reach to the minimal potential energy and the correct parameter value cannot be obtained.

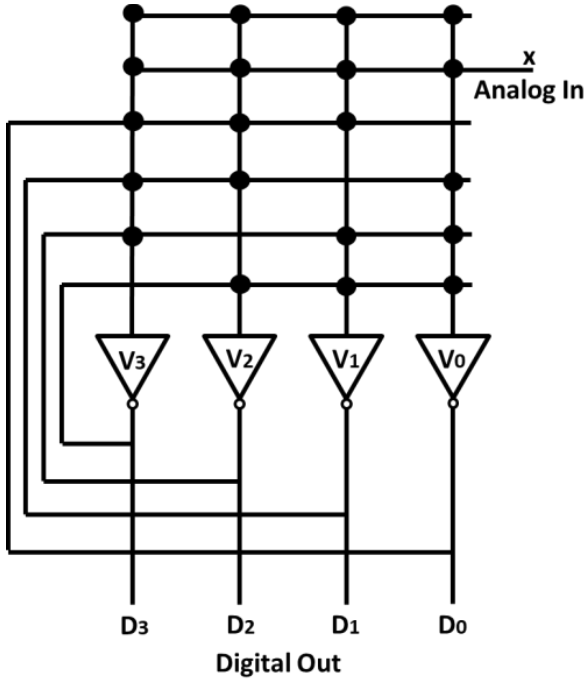


Fig. 1. Traditional Hopfield neural network ADC.

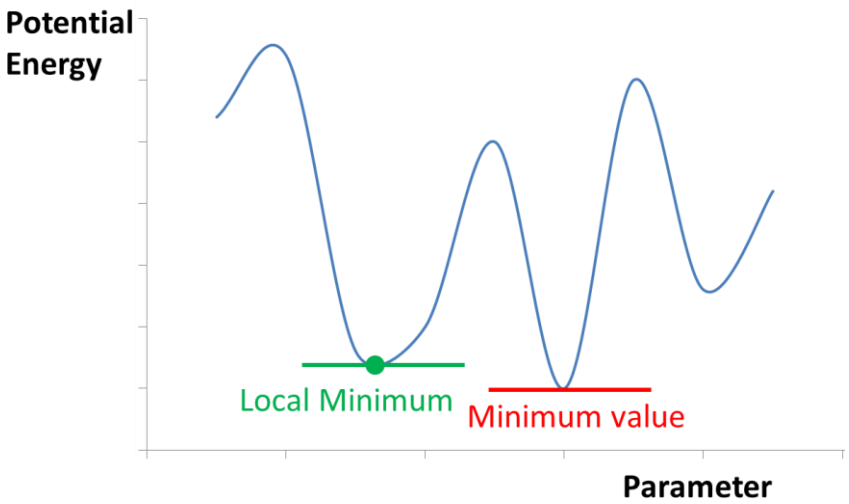
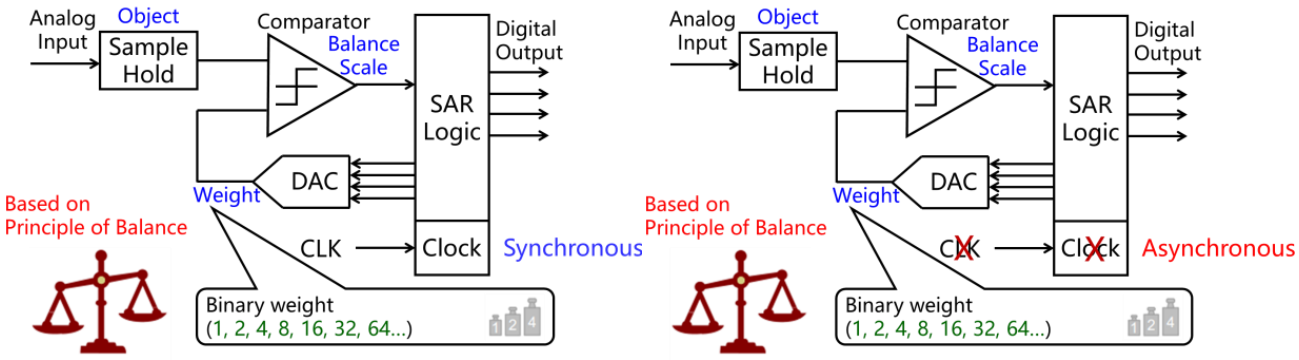


Fig. 2. Problem of local minima. The vertical axis shows potential energy and the horizontal axis shows parameters.

3. Proposed Hopfield Network ADC

3.1 Binary Asynchronous SAR ADC

Fig. 3 (a) explains the binary-weighted synchronous SAR ADC while Fig. 3 (b) illustrates the asynchronous one. A typical 10-bit 150 MHz synchronous SAR ADC requires 1.8GHz (= (10+2) x 150MHz) clock internally, while asynchronous one needs only 150MHz clock for the sampling of the input data at the sampling circuit in front of the SAR ADC; this is an advantage of asynchronous one. Notice that the sampling speed of the asynchronous SAR ADC in Fig. 1 is determined by the time constant of the resistors and the associated parasitic capacitors.



(a) (b)

Fig. 3. Binary weighted SAR ADC. (a) Synchronous one. (b) Asynchronous one.

Our improved Hopfield network asynchronous SAR ADC is shown in Fig. 4; this is the 6-bit case, but extension to higher bit case is straightforward. The network in Fig. 4 discards feedback paths from lower bits to higher bits and uses all feed forward configuration; then there is no local minimum. Also notice that the inverter circuit is used as a comparator. The advantages of the Hopfield network asynchronous SAR ADC are fast operation, no high frequency internal clock, no SAR logic and very simple design.

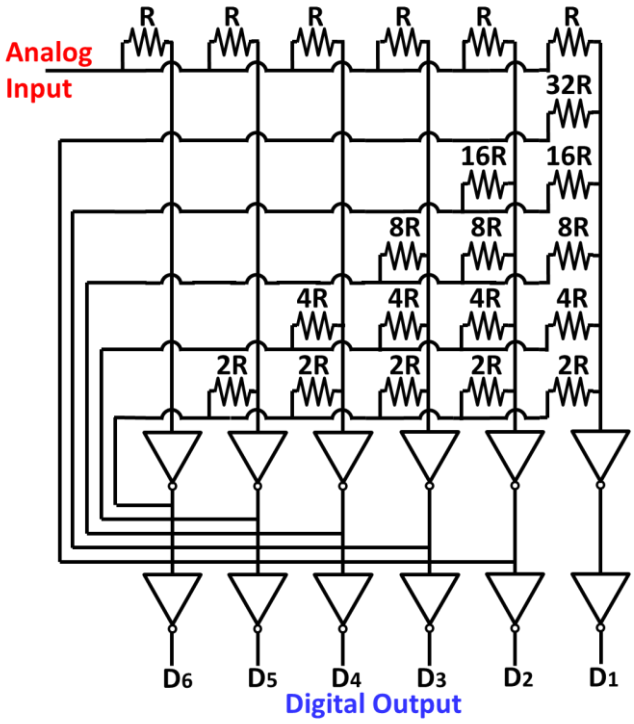


Fig. 4. Investigated binary-weighted asynchronous SAR ADC based on improved Hopfield network in 6-bit case.

We have investigated a 10-bit binary-weighted SAR ADC in Fig. 4 and we have the following decimal digital output from the inverter outputs of D_{10}…. D_1:

$$Data = \left(\frac{1}{R_{10}}\right)D_{10} + \left(\frac{1}{R_9}\right)D_9 + \left(\frac{1}{R_8}\right)D_8 + \left(\frac{1}{R_7}\right)D_7 + \left(\frac{1}{R_6}\right)D_6 + \left(\frac{1}{R_5}\right)D_5 + \left(\frac{1}{R_4}\right)D_4 + \left(\frac{1}{R_3}\right)D_3 + \left(\frac{1}{R_2}\right)D_2 + \left(\frac{1}{R_1}\right)D_1$$

Here $\frac{1}{R_{10}} = 512, \frac{1}{R_9} = 256, \frac{1}{R_8} = 128, \frac{1}{R_7} = 64, \frac{1}{R_6} = 32, \frac{1}{R_5} = 16, \frac{1}{R_4} = 8, \frac{1}{R_3} = 4, \frac{1}{R_2} = 2, \frac{1}{R_1} = 1.$

SPICE simulation results are shown in Fig.5, and the operation of the 10-bit binary-weighted asynchronous SAR ADC has been confirmed, as shown in Fig. 6.

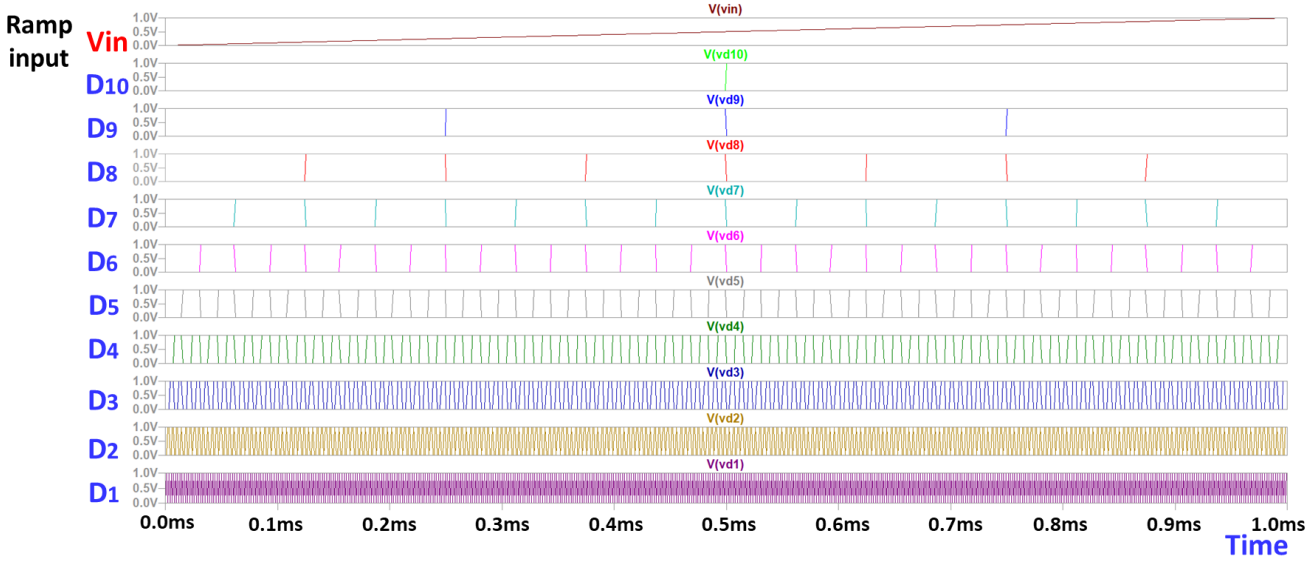


Fig. 5. SPICE simulation results of
the10-bit binary-weighted asynchronous SAR ADC with the improved Hopfield network.

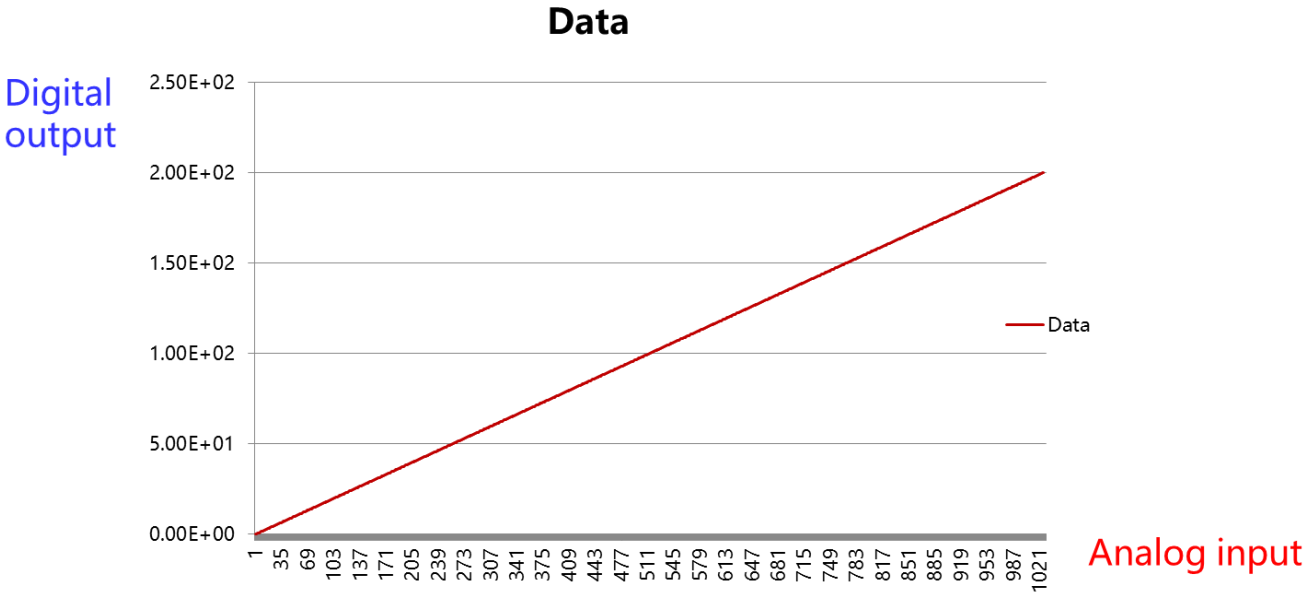


Fig. 6. Decimal data calculation result of 10-bit binary-weighted SAR ADC.

Each inverter used as a comparator in Fig. 4 is composed of a PMOS and an NMOS with VDD=1.0V and VSS=0.0V, and hence the analog input is swept from 0 to 1.0V in Fig.5.

3.2 Non-binary Asynchronous SAR ADC

Fibonacci sequence definition is given as follows:

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Then Fibonacci numbers are given as follows:

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, \ldots$$

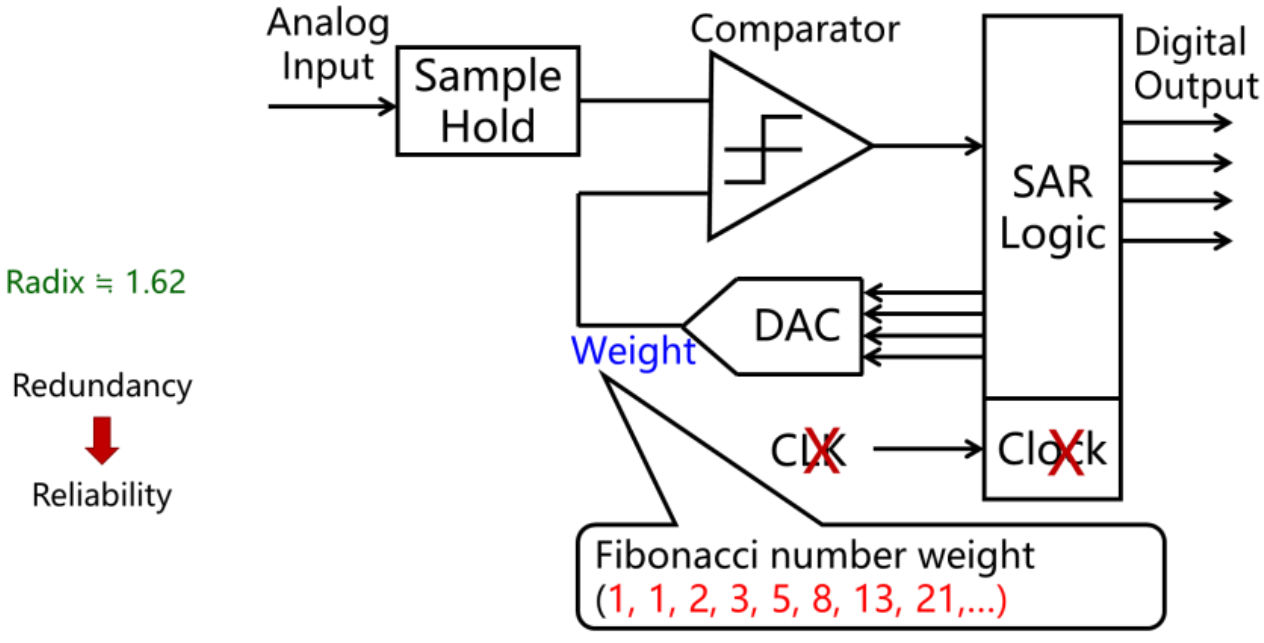
Notice that the radix of the Fibonacci number sequence is approximately 1.62. Hence, by using Fibonacci number weights, non-binary weight SAR ADC with the radix of approximately 1.62 can be realized. Fig. 7 (a) explains the Fibonacci number weighted asynchronous SAR ADC conceptually while Fig. 7 (b) shows its implementation with the improved Hopfield network. Also notice that the non-binary weighted SAR ADC including the Fibonacci number weighted SAR ADC is discussed in [5, 6, 7].

We have the following decimal digital output from the inverter outputs of $D_{10} \ldots D_1$ in the improved Hopfield network ADC:

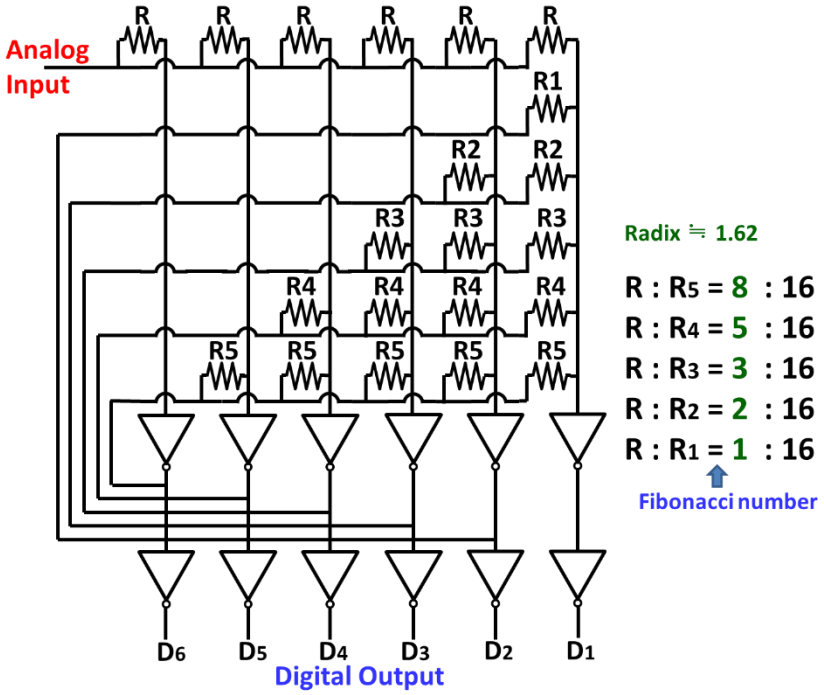
$$Data = \left(\frac{1}{R_{10}}\right) D_{10} + \left(\frac{1}{R_9}\right) D_9 + \left(\frac{1}{R_8}\right) D_8 + \left(\frac{1}{R_7}\right) D_7 + \left(\frac{1}{R_6}\right) D_6 + \left(\frac{1}{R_5}\right) D_5 + \left(\frac{1}{R_4}\right) D_4 + \left(\frac{1}{R_3}\right) D_3 + \left(\frac{1}{R_2}\right) D_2 + \left(\frac{1}{R_1}\right) D_1 \quad (2)$$

Here $\frac{1}{R_{10}} = 89, \frac{1}{R_9} = 55, \frac{1}{R_8} = 34, \frac{1}{R_7} = 21, \frac{1}{R_6} = 13, \frac{1}{R_5} = 8, \frac{1}{R_4} = 5, \frac{1}{R_3} = 3, \frac{1}{R_2} = 2, \frac{1}{R_1} = 1,$

SPICE simulation results are shown in Fig. 8, and the operation of the 10-bit Fibonacci number weighted SAR ADC has been confirmed, as shown in Fig. 9.



(a)



(b)

Fig. 7. Fibonacci number weighted asynchronous SAR ADC. (a) Conceptual explanation. Implementation with the improved Hopfield network (6-bit case).

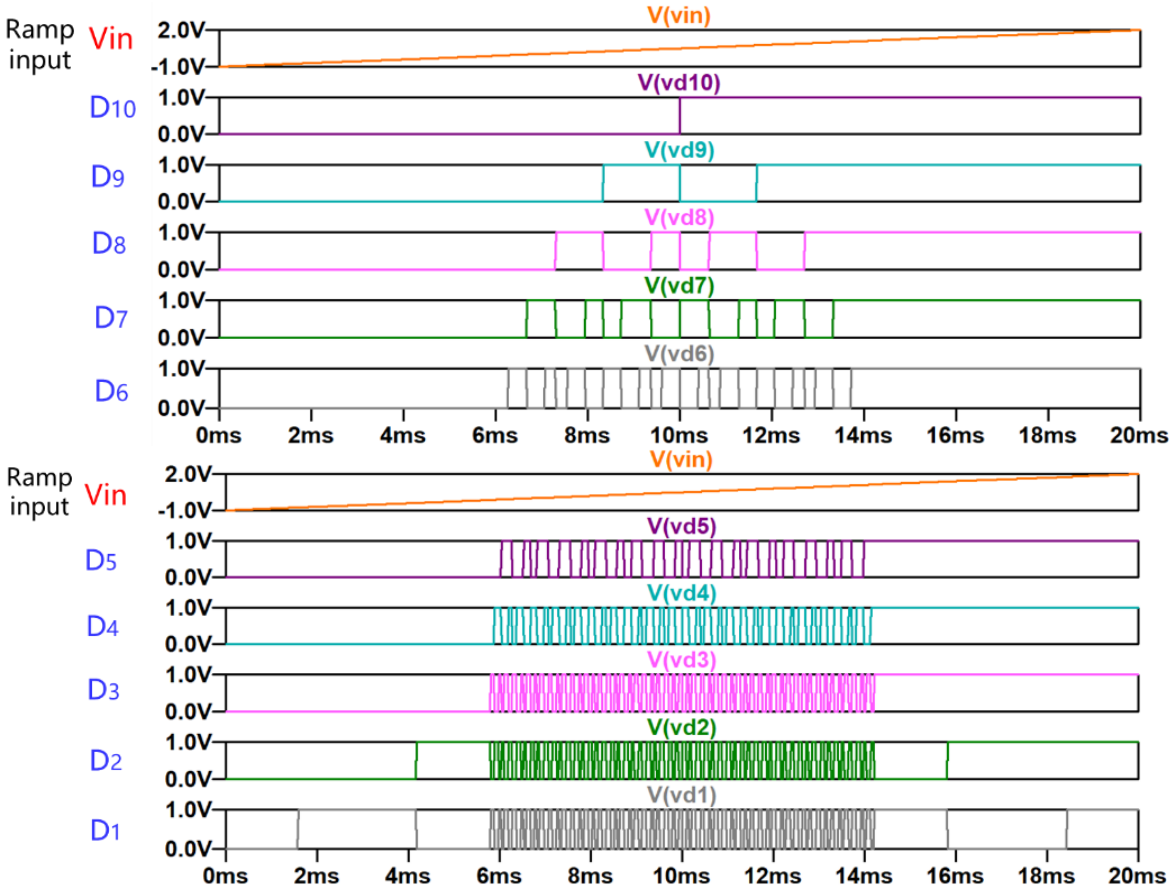


Fig. 8. SPICE simulation results of the 10-bit Fibonacci number weighted asynchronous SAR ADC based on the improved Hopfield network.

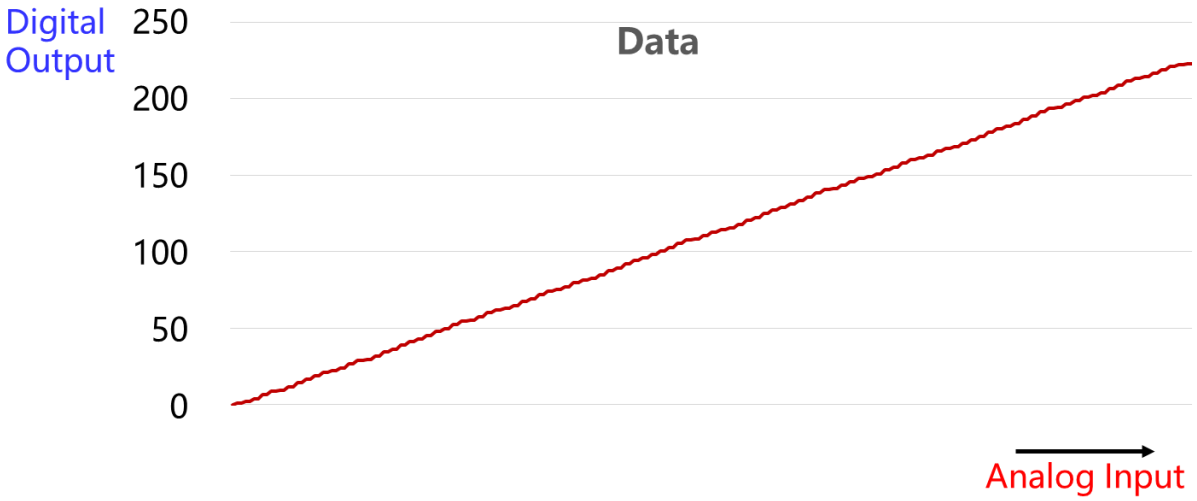


Fig. 9. Decimal data calculation of the10-bit Fibonacci number weighted asynchronous SAR ADC based on the improved Hopfield network.

Each inverter used as a comparator in Fig. 7 is composed of a PMOS and an NMOS with V_{DD}=1.0V and V_{SS}=0.0V, but in order to see the effects of the wide range analog input for the Fibonacci number weighted SAR ADC, it is swept from -1.0 to 2.0V in Fig.8.

3.3 DAC Array inside Improved Hopfield Network ADC

Fig. 10 shows the resistive network DAC and its SPICE simulation result and Fig. 11 explains that the improved Hopfield network ADC has a DAC array.

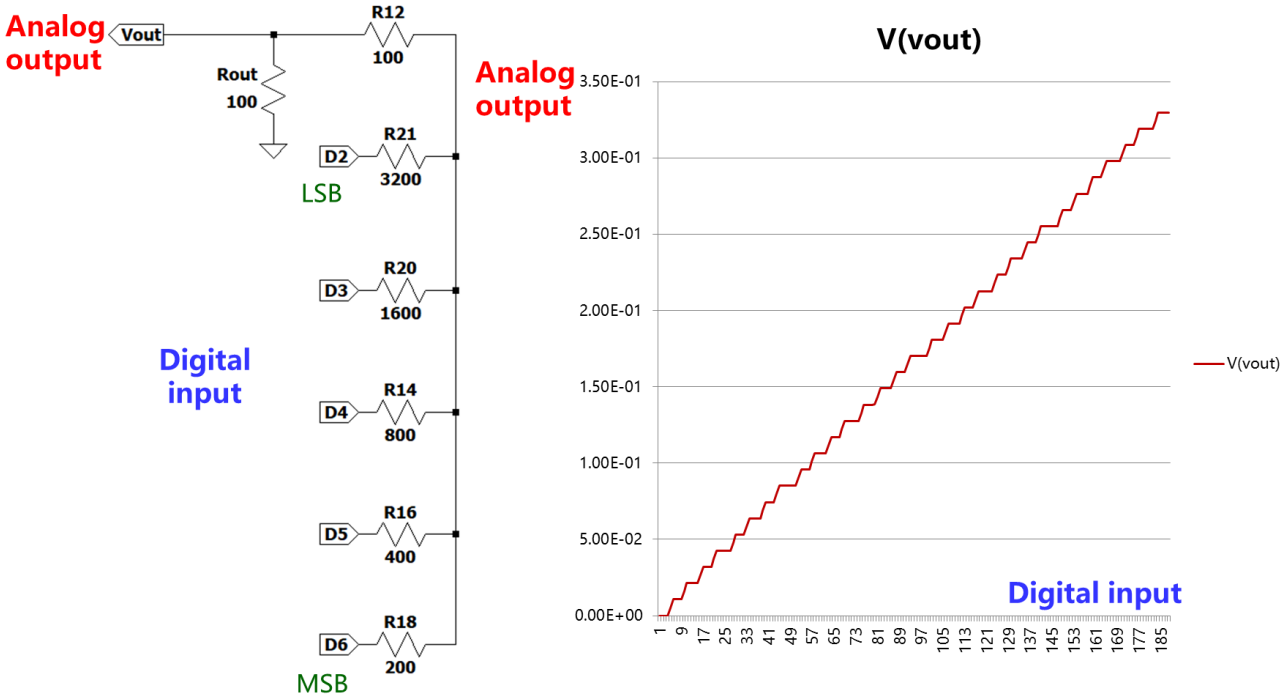


Fig. 10. DAC inside the Hopfield network

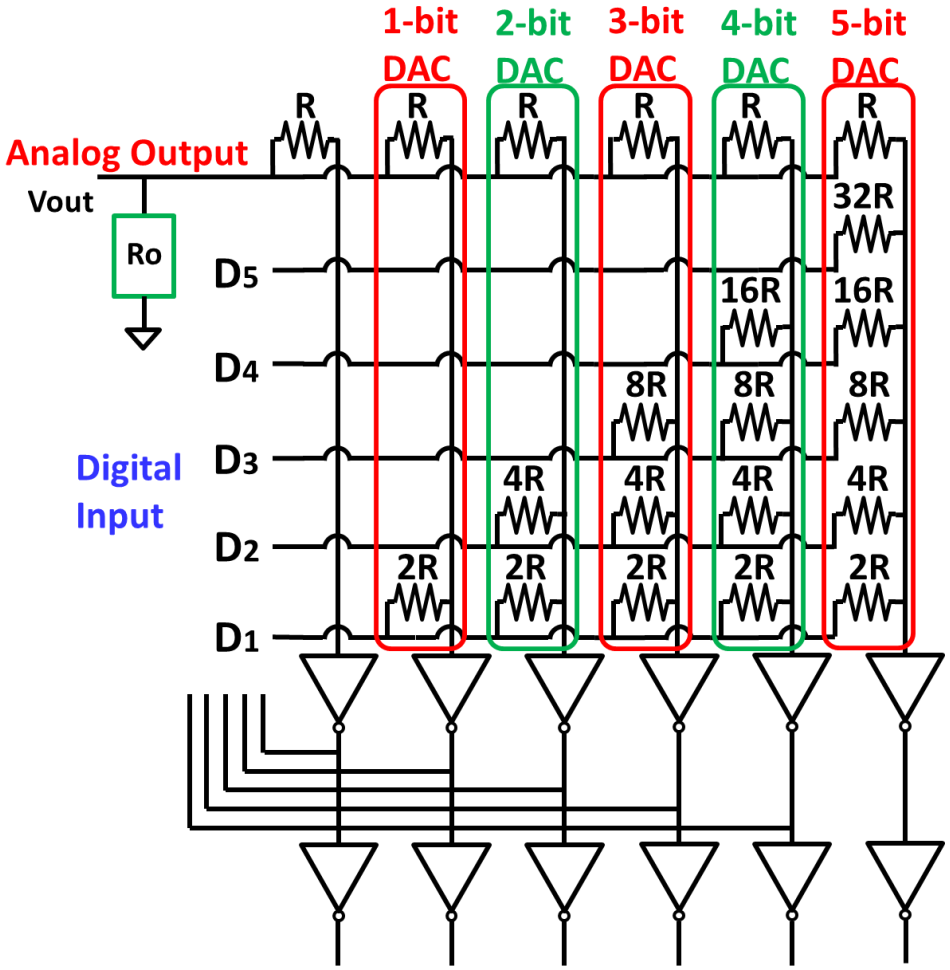


Fig. 11. DAC array inside the improved Hopfield network

4. Conclusion

This paper has proposed an improved Hopfield network ADC which does not have feedback paths from lower bits to higher bits. It can avoid the local minima problem and realize an asynchronous SAR ADC with the following advantages: very fast operation, simple design, non-binary as well as binary configurations. Its operation was verified with SPICE simulations. Technology development of large resistors with good matching and small chip area is expected for the proposed SAR ADC to be competitive to the state-of-the-art SAR ADC.

We conclude this paper by remarking that our proposed Hopfield network ADC can be used as a stand-alone SAR ADC competitive to its state-of-the-art, but one of its killer applications would be the multi-bit ADC inside the ΔΣ AD modulator, where high-speed and low-power are mandatory but the nonlinearity due to device mismatches (such as inverter threshold voltage variations) does not matter, thanks to the noise-shaping effects of the modulator [8, 9].

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