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Proactive Use of Finite Aperture Time in Sampling Circuit for Sensor Interface

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Abstract. This paper describes the use of the finite aperture time in the sampling circuit for effective low pass filtering, targeted for sensor interface applications. In IoT systems, a lot of sensors are used and their output signals are in the low frequency band. Their associated high frequency noises are low-pass filtered, and then they are sampled and AD converted. The low-pass filter often requires large chip area We consider here to use the finite aperture time for low-pass filtering by making the sampling clock slope gentler for the sampling circuit; this can be implemented with small chip area. We also show in SPICE simulation that the long aperture time reduces the pedestal output voltage error of the sampling circuit due to the MOS switch charge injection and clock feedthrough.

1. Introduction

Countries all over the world are developing renewable energy and small electronic systems can operate with low energy. However, the presence of noise in small electronic systems cannot be ignored in many applications. The purpose of this research is to reduce the noise existing in the small electronic system for energy harvesting based on the electronic circuit design, and to improve the signal acquisition accuracy and efficiency of the sensor interface circuits in IoT systems, where the signal components are in the low frequency bands while the noises are in the high frequency. As we all know, the sampling circuit is used for the waveform acquisition, which enables the following ADC to perform AD conversion with high accuracy [1].

This research is based on a sampling circuit (Fig. 1) combined with finite aperture time control for reduction of the noise and the pedestal error due to charge injection and clock feedthrough, targeted for sensor interface analog front-end circuits [2]. Figs. 2 and 3 explain the aperture time in the sampling circuit. We confirm the conjecture through quantitative analysis of aperture time that slowly closing the switch of the sample hold circuit can reduce the circuit noise and also the pedestal error [3].

Aperture time is the inverse of the camera shutter speed. As shown in Fig.4, when the shutter is fast enough, we can clearly see the high-speed moving reference object in dark and fuzzy background. On the other hand, when the shutter is slow enough, the background becomes clear and bright although the moving reference object becomes blurred. This gives rise to two types of cameras: high-speed shutter cameras and slow shutter cameras. Using the characteristics of the aperture time can effectively reduce the amplitude of the signal, reduce noise, and improve some sensor-related product quality.

Notice that in the wideband signal acquisition, the finite (non-zero) aperture time is a problem because it works as low pass filtering and the high frequency signals are blurred [4-10]. However, here we propose use it proactively in the sensor interface circuit, where the signal components are in

the low frequency band and high frequency noise components should be removed. In other words, we argue the statement that for high frequency signal acquisition, the short aperture time is desirable, whereas for low signal acquisition, the long aperture time is better in the sampling circuit.

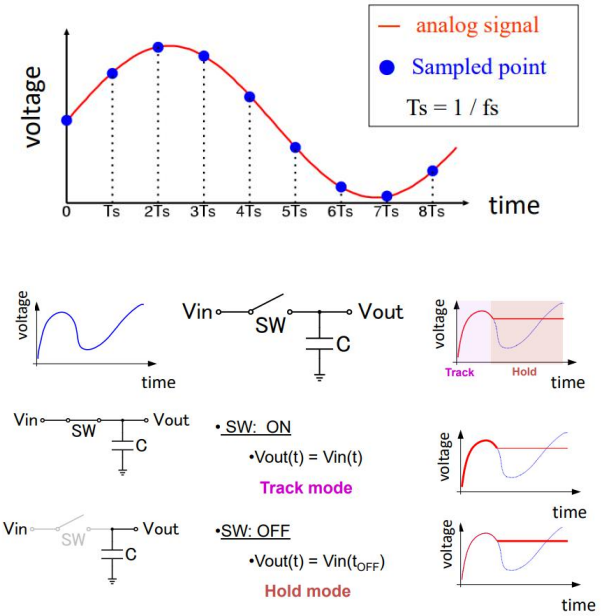

Fig. 1 Waveform sampling and sampling circuit.

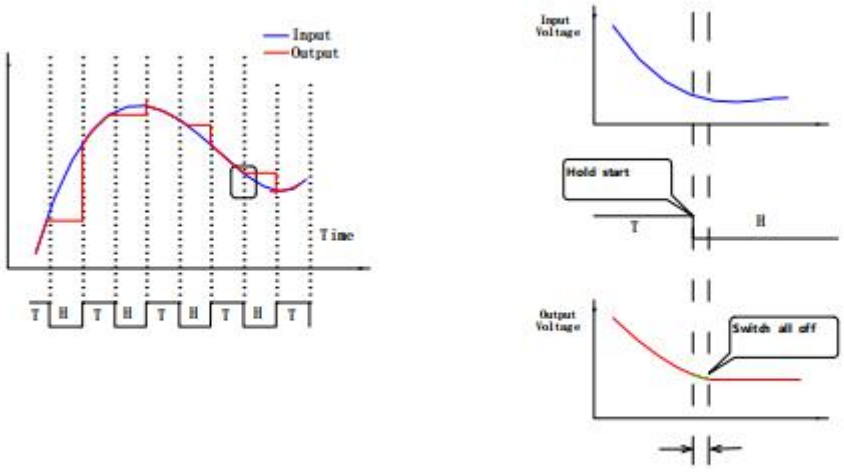

Fig. 2 Definition of aperture time in a sampling circuit.

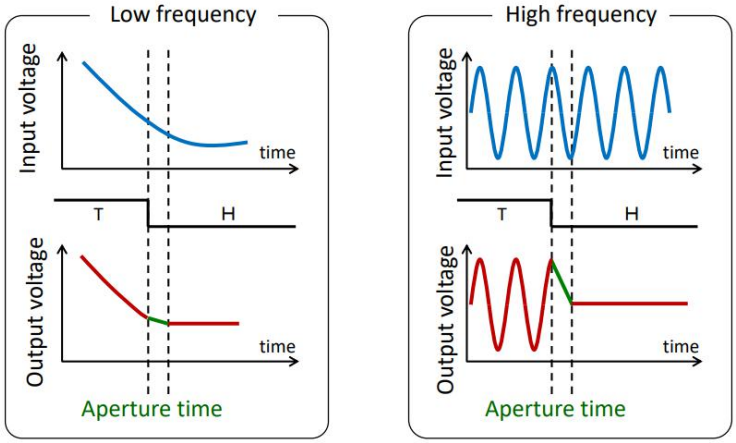

Fig. 3 Finite aperture time effects for low signal and high frequency signal sampling.

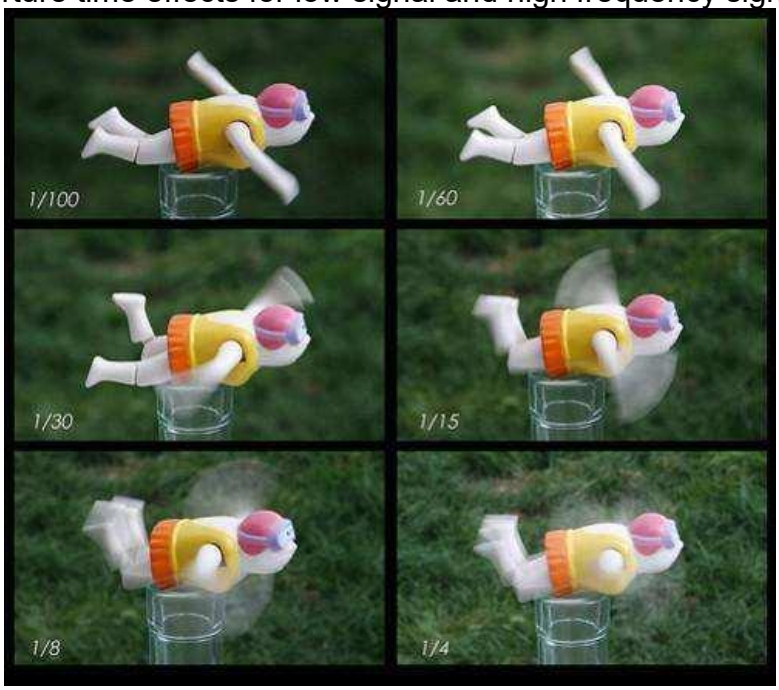

Fig. 4 Captured moving object and background for various shutter speeds.
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2. Low Pass Filtering Effect of Aperture Time in Sampling Circuit

The definition of the aperture time is the integral of the time when the switch starts from closing to fully open (Fig. 2). We have derived analytically in [4-7] that for the sampling circuit model in Fig. 5, the finite aperture time shows the low pass action as follows:

$$\frac{V_C}{V_{in}} = \frac{sinc(\omega\tau_2)}{sinc(\omega\tau_2) + j\omega\tau_1}$$

Here τ_1= RC.

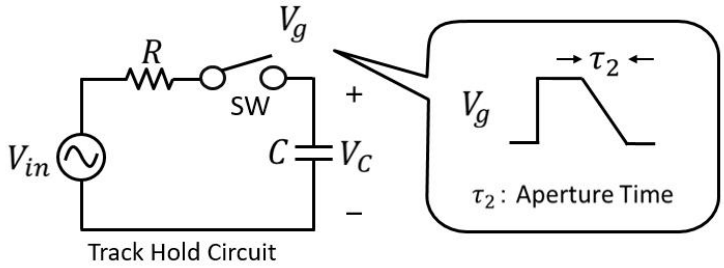

Fig. 5 Sampling circuit model with finite aperture time τ_2 and switch on-resistance R.

The detailed discussions on the circuit in Fig. 5 including the rigorous definition of the effective aperture time are shown in [4-9], though these are from the viewpoint of the wideband signal sampling instead of the high frequency noise reduction.

We consider here that the hold capacitor value of C is determined by kT/C noise, and if the value of R is increased for low-pass filtering, the settling time of the sampling circuit becomes longer; hence the proactive usage of the finite aperture time is effective as the total circuit performance balance.

3. Charge Injection Reduction of Finite Aperture Time in Sampling Circuit

This section discusses the finite aperture time effects to the charge injection of the MOS switch in the sampling circuit using SPICE simulation with TSMC 0.1μm CMOS parameters.

Fig. 6 explains the charge injection of the NMOS switch. Fig. 6 (a) shows the channel electrons when the NMOS switch is on, whereas Fig. 6 (b) shows the case that it turns off; some of the channel electrons are dispelled into the source from the channel and the others are into the drain. The balance of the charge redistribution to the source and drain sides depends on their associated impedances. When a hold capacitor is connected to the drain, its voltage is dropped by ΔV_{OUT} as shown in Fig. 7 where ΔV_{OUT} is denoted as ΔV_a or ΔV_b. This ΔV_{OUT} is called as the pedestal error of the sampling circuit. The pedestal error is mainly caused by the charge injection and the clock feedthrough [12]. We found by SPICE simulation that the pedestal error is reduced for long aperture time, which is beneficial for low frequency signal acquisition with low aperture time sampling.

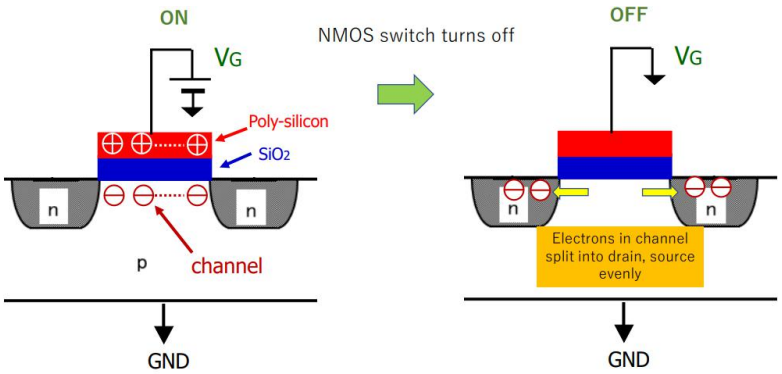

Fig. 6 Channel charge of NMOS. (a) ON state. (b) Turn off transition.

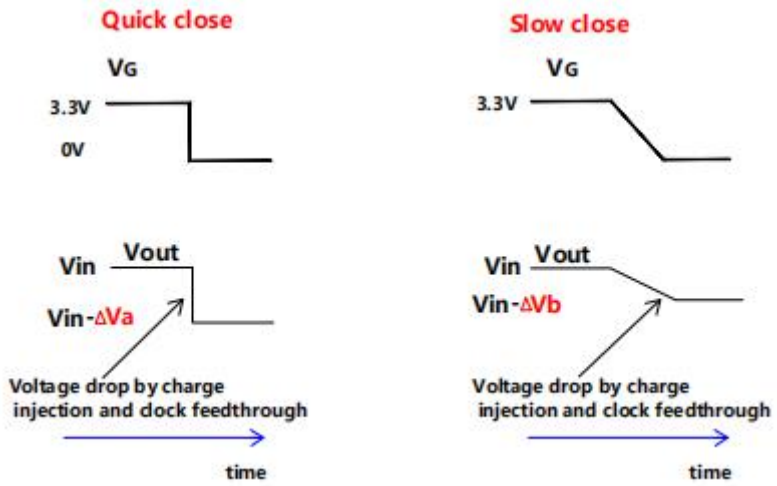

Fig. 7 Charge injection in sampling circuit for quick and slow turn off.

4. Simulation Results of Pedestal Error in Sampling Circuit

We have simulated the pedestal error in MOS sampling circuit in various cases, using TSMC 0.18μm BSIM3v3 parameters. We set the default parameters as W=20μm L=0.2μm for the MOS switch, C=0.1pF of the hold capacitor, Tfall=0.01ns of the sampling clock fall time which corresponds to the aperture time, and Vdd=3.3V of the power supply.

Our simulation results show the following:

(1) As W increases, ΔV_{OUT} increases (approximately in proportion).
(2) As L increases, ΔV_{OUT} increases (approximately in proportion).
(3) As C increases, ΔV_{OUT} decreases (approximately in inverse proportion).
(4) As Tfall increases, ΔV_{OUT} decreases, as shown in Figs. 8. 9.
(5) ΔV_{OUT} difference between NMOS and PMOS switch cases is small, as shown in Fig.10.

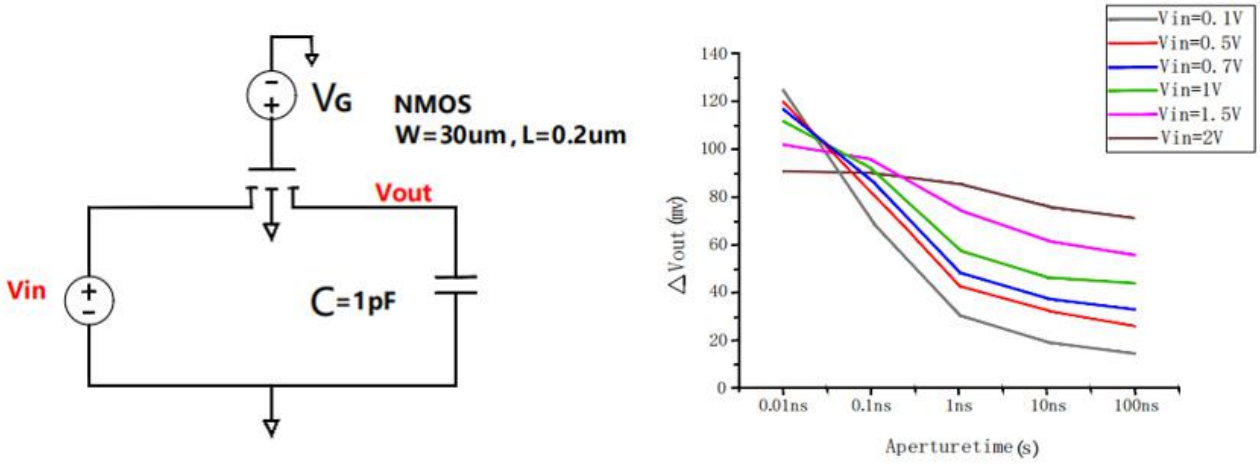

Fig. 8 Pedestal error in NMOS switch sampling circuit for various aperture time.

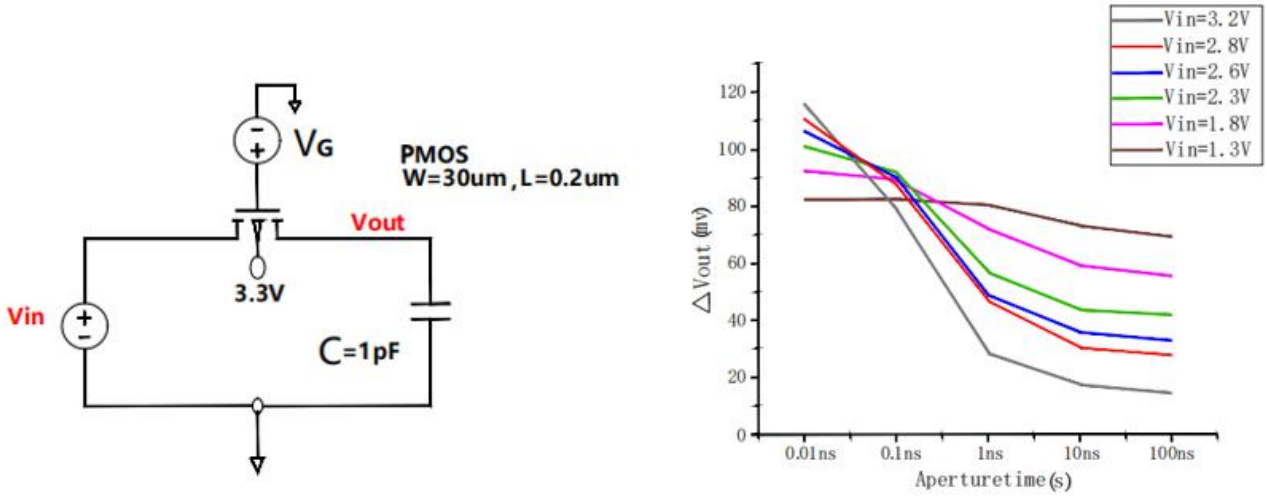

Fig. 9 Pedestal error in PMOS switch sampling circuit for various aperture time.

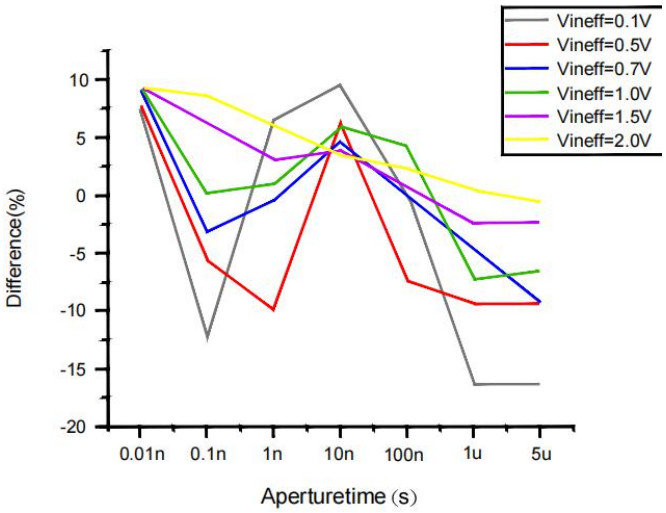

Fig. 10 Difference of pedestal errors between NMOS and PMOS switch sampling circuits. *Vineff* is defined as *Vin* for NMOS switch sampling circuit, while *Vdd-Vin* for PMOS one.

5. Conclusion

In this paper, we have considered to use the finite aperture time in the sampling circuit proactively to reduce the noises, targeted for the sensor interface applications. We have found by SPICE simulation that the charge injection is also reduced in the MOS sampling circuit. As the next step, we will explain the reasons for this charge injection reduction by the slow turn off, based on MOS modeling and physics [13, 14].

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