Proceedings of International Conference on
Technology and Social Science 2018 (ICTSS 2018)
INVITED

Output Voltage Ripple Correction with Spread Spectrum Using Frequency Modulation for Switching Converters

Yasunori Kobori[a], Natsuko Miki[b],Yifei Sun[c],
Nobukazu Tsukiji[d] and Haruo Kobayashi[e]

Division of Electronics and Informatics, Gunma University, 1-5-1 Tenjin-cho, Kiryu 376-8515, Japan

[a]< kobori@gunma-u.ac.jp >, [b]< @t13304917@gunma-u.ac.jp >,[c]< t172d004@gunma-u.ac.jp >,
[d] < ntsukiji@gunma-u.ac.jp >, [e] < koba@gunma-u.ac.jp >

Keywords: switching converter, noise spread spectrum, EMI reduction, output ripple correction

Abstract. This paper explains the reduction method of the output voltage ripple for the buck-type switching DC-DC converter which uses the linear swept frequency modulation to reduce the EMI noise in the spread spectrum. When the clock frequency of the control circuit is modulated with the linear sweep signal like the triangle signal, the spectrum level of the clock frequency decreases in proportion to the amplitude of the modulation signal. But inversely proportional to that, the output voltage ripple increases, that is undesired for the converter.

We have proposed the reduction technology of the output voltage ripple using the modulation of the slope of the saw-tooth signal which is used for generating the PWM pulse to drive the main power switch. In order to modulate the saw-tooth slope, auxiliary current flows to the saw-tooth generator in proportion to the voltage of the modulation signal.

1. Introduction

For a switching converter, it is the aim to provide the stable voltage source to the system. But it has always the problem about the Electro-Magnetic Interference (EMI) noise. To reduce the EMI noise of the clock frequency, it is well known to modulate the clock frequency (or phase). When the level of the modulation signal is largely set, the spectrum level of the clock frequency is much reduced. At the same time, unfortunately, the output voltage ripple much increases, it is no good for the switching converter. This paper shows the technique to reduce the spectrum level without increase of the output ripple by correcting the slope of the saw-tooth signal according to the modulation level.

2. Switching Converter and Spread Spectrum of EMI Noise

2.1 Buck Converter and its Operation [1]

In this paper, the buck-type DC-DC switching converter is used shown in Fig. 1. This converter consists of the power stage and the control part. The power stage consists of the main switch, the freewheel diode, the inductance and the output capacitance. The control part consists of the operational amplifier, the comparator and the saw-tooth generator which is triggered by the clock pulse. In this figure, the clock oscillator is modified by the modulation signal to reduce the EMI noise. Of course, in the normal converter, the oscillator is not modified.

Figure 2 shows the operating signals of this converter. The output voltage Vo is compared with the reference voltage Vref and amplified to provide the voltage error ⊿V. Comparing this error voltage

with the saw-tooth signal (SAW), the PWM (pulse width modulation) signal is generated to drive the main switch. The output voltage ripple Vo is about 2 mV in this converter.

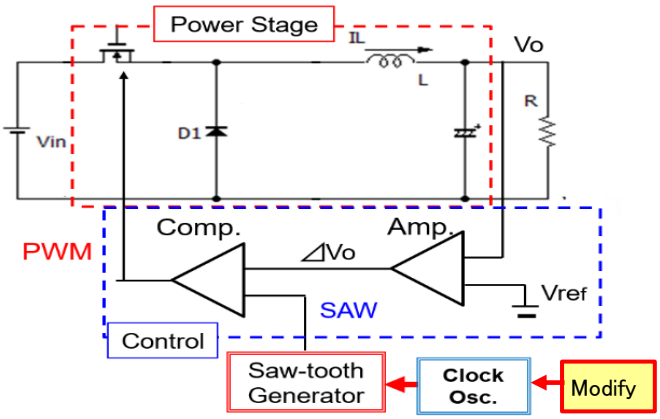

Fig. 1. Buck Type Switching Converter

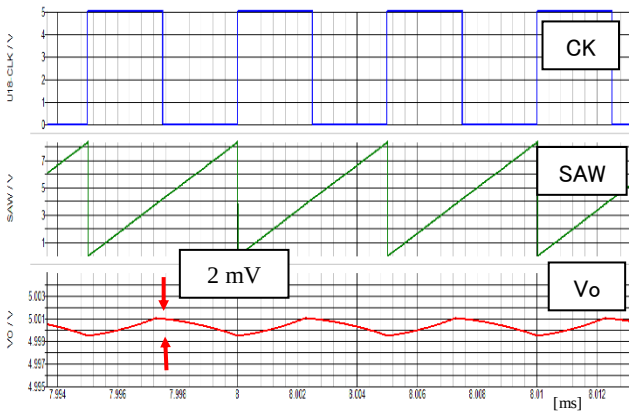

Fig. 2. Major Waveform of Converter

2.2 Spread Spectrum of EMI Noise with Frequency Modulation [2]

Figure 3 shows the spread spectrum of the PWM signal without the clock modulation. By modifying the clock frequency with the voltage controlled oscillator (VCO), the peak level of the clock frequency in the spectrum is reduced shown in Fig. 5. In this case, the modulation signal, shown in Fig. 4, uses the sine wave, which has 2 kHz frequency and 0.5V amplitude. The period of the clock pulse is modulated and the peak of the SAW signal is waved and the output ripple increases to 20 mV shown in Fig.4. Increasing the amplitude of the modulation signal to Vm=2.0V, the peak level of the clock frequency spectrum decreases from 0.9V to 0.5V which is -5.1dB reduction. Here we use the simulation software SIMetrix/SIMPLIS.

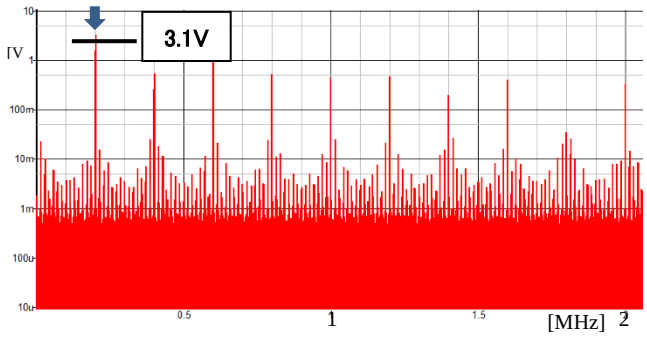

Fig. 3. Spectrum w/o Modulation

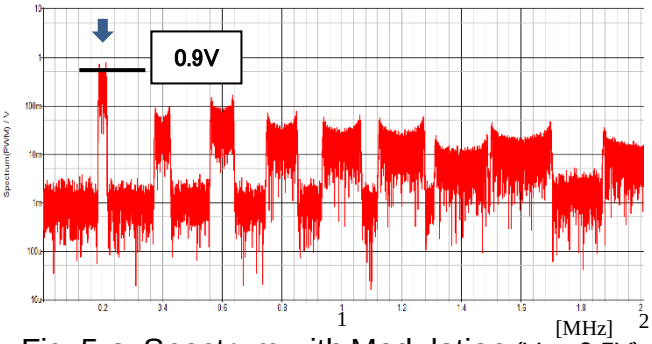

Fig. 5-a. Spectrum with Modulation (Vm=0.5V)

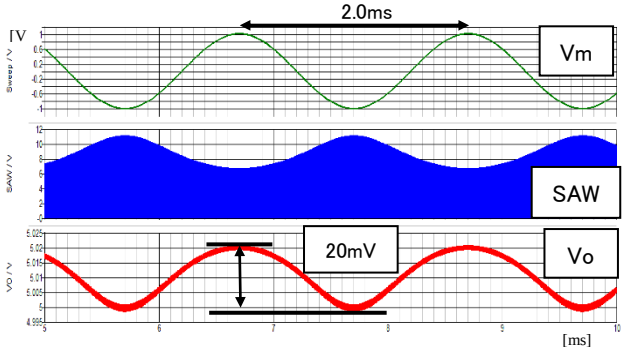

Fig. 4. Ripple with Modulation(Vm=2.0v)

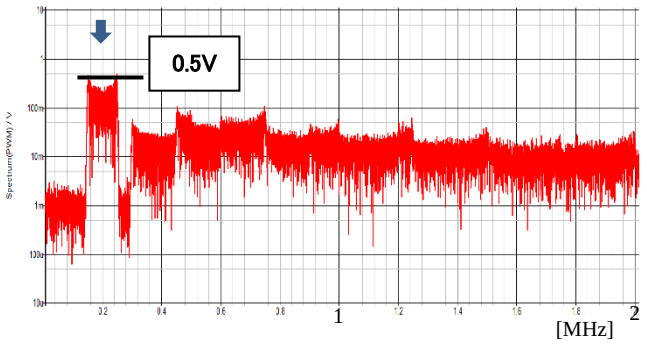

Fig. 5-b. Spectrum with Modulation(Vm=2.0V)

The parameters of this converter and the conditions of the VCO are shown in Table1 and Table 2.

Table 1 Parameters of Converter

Input Voltage	Vin	12.0	[V]
Output Voltage	Vo	5.0	[V]
Output Current	Io	0.50	[A]
Inductance	Lo	200	[uH]
Capacitance	Co	220	[uF]
Clock Frequency	Fck	200	[kHz]

Table 2 Conditions of VCO & SAW

Sensitivity	50	[kHz/V]
Base Voltage	4.0	[V]
Modulation V	0.5～2.0	[V]
Modulation Freq.	0.5～2.0	[kHz]
SAW Current	2.0	[mA]
SAW Capacitance	1.2	[nF]

2.3 Transfer Function and Frequency Characteristics of Output Ripple

The open-loop transfer function of this converter without the clock modulation is shown in Fig. 6. The peak frequency is about 0.8kHz and the zero-cross frequency in the gain curve is 14 kHz. The frequency characteristic of the output ripple with the clock modulation depends on the closed-loop characteristic shown in Fig. 7, in which the peak is about 15 kHz. When the frequency of the modulation signal is set higher than 20 kHz, the ripple is less than 20mV. In this case, the amplitude of the modulation signal is set at Vm=2.0V.

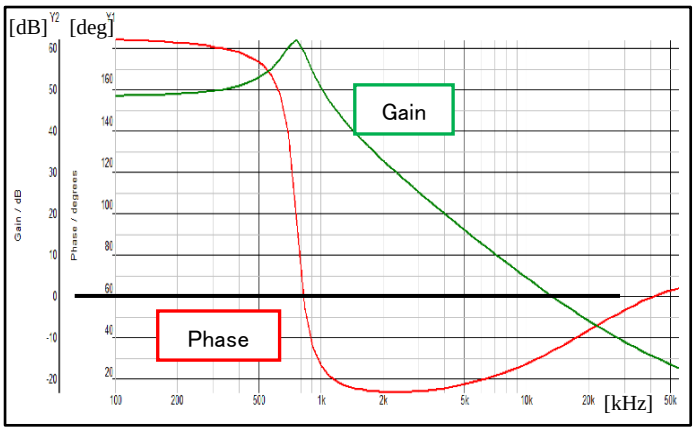

Fig. 6. Open-Loop Transfer Function

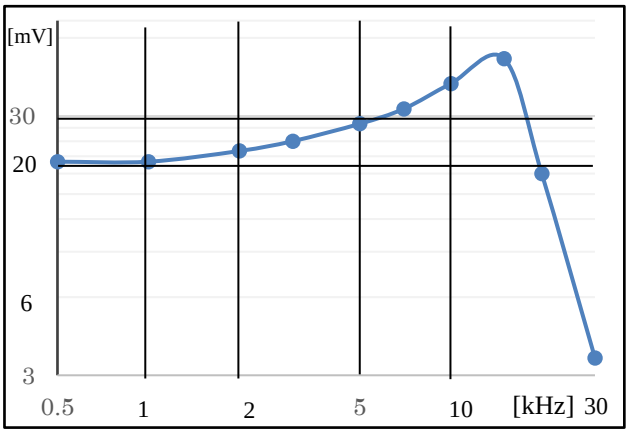

Fig. 7. Frequency Characteristic of Ripple

3. Proposed Output Voltage Ripple Correction Method

3.1 Relationship between Modulation Level and Output Ripple

According to the amplitude of the modulation signal, the peak level of the clock frequency spectrum decreases in reverse proportion to the modulation level shown in Fig. 8. On the other hand, the output voltage ripple is linearly increases shown in Fig. 9. In this case, the clock frequency is 200kHz and the modulation frequency is 2.0kHz, respectively.

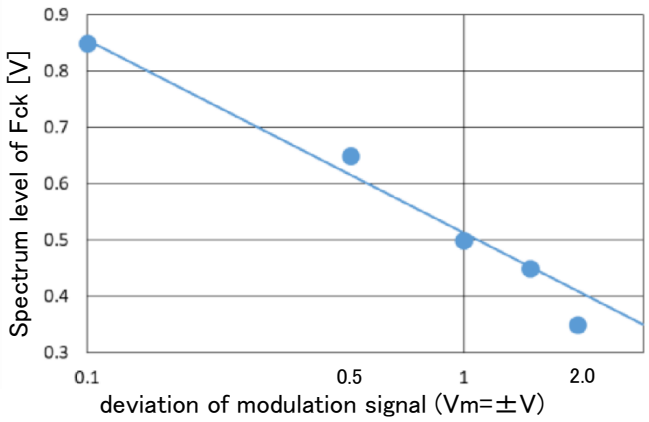

Fig. 8. Spectrum Level vs. Modulation Level

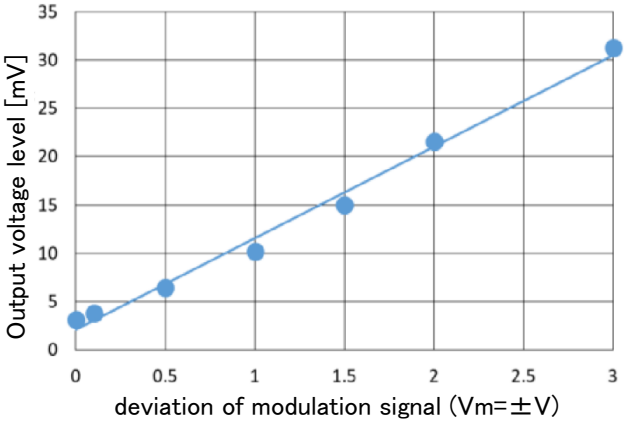

Fig. 9. Output Ripple vs. Modulation Level

3.2 Correction Method of Output Ripple [3]

The output voltage ripple is in proportion to the amplitude of the modulation signal. Considering the relationship with the modulation level and the duty ratio D of the PWM pulses, the PWM pulses almost keep its pulse width, but the period of the PWM pulse is a little changed by the modified signal. The sensitivity of the VCO is 50kHz/V and the basic DC controlled voltage is Vb=4.0V. The modulation signal is triangular, which is Fm [kHz] and Vm [V] amplitude, respectively. The change of the clock frequency is expressed like Eq. (1). In this case, the deviation of the duty ratio D of the PWM pulse is derived like Eq. (2).

$$Fck= 50k\cdot(Vb+Vm)=200k+50k\cdot Vm \tag{1}$$

$$D'=Do+\triangle D=Do/(1-\alpha)\fallingdotseq Do(1+\alpha) \tag{2}$$

Therefore the variation of the duty $\triangle D$ is expressed bellow.

$$\triangle D=\alpha Do= 2(Vm/Vb)/(Fck/Fm) \tag{3}$$

Considering the equations (1) ~ (3), the clock modification makes the small change of the duty ratio, which makes the output ripple large. So, it is reasonable to compensate the change of the duty ratio in order to correct the output ripple. To do this compensation, the slope of the saw-tooth is compensated by the additional current source according to the modified signal shown in Fig.10 and 11.

The number of the clock N in the half of the period Tm is derived as Eq. (4). When the relationship between the additional current and the modulation amplitude Vm is expressed like Eq. (5), the current compensated ratio per a clock cycle is derived as Eq. (6). To correctly compensate the output ripple, set $\alpha Do= dI_{SAW}$, that is Eq. (3) =Eq. (6). Then the conductance G of the additional current source is expressed like Eq. (7). Here the I_{SAW} is the original current source of the SAW generator, the unit [S] of G is "Siemens". Adapting the parameters in Table 1, G=2mA/4V=500 [uS].

$$N=(Tm/2)/Tck=0.5\cdot Fck/Fm \tag{4}$$

$$\triangle I_{SAW} =G\cdot Vm \tag{5}$$

$$dI_{SAW} =(\triangle I_{SAW} /I_{SAW})/N$$

$$=(Vm\cdot G/I_{SAW})/(0.5\cdot Fck/Fm)=2VmG/(I_{SAW}\cdot Fck/Fm) \tag{6}$$

$$G= I_{SAW}/Vb\ [S] =2mA/4V=500\ [uS] \tag{7}$$

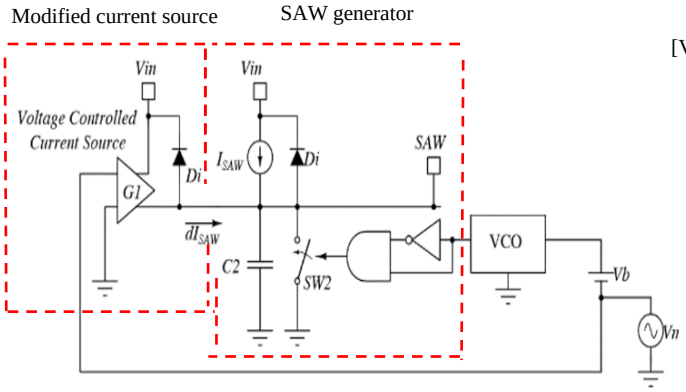

Fig. 10. SAW Generator & Modified Circuit

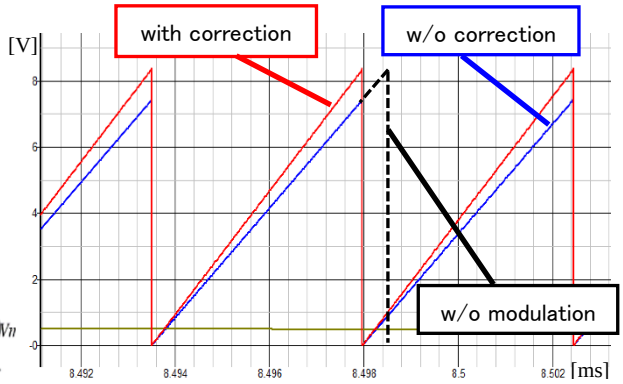

Fig. 11. Comparison of SAW Signals

3.3 Simulation Result of Output Ripple Correction

The output voltage ripple without modulation, which we call the static ripple, is usually 2 mv in this converter shown in Fig. 2. By modulating the clock, the ripple increases to 20 mV, which we call the modulated ripple, shown in Fig. 4. This increased ripple is reduced with the compensation described above. Figure 12 shows the compensated ripple with the various additional current source which is shown in Eq. (7). In Fig. 12, the larger the conductance G becomes, the smaller the modulated ripples change. When the conductance G becomes lager than 500 uS, the phase of the ripple inverts and the ripples increase. Figure 13 shows the relationship between the conductance G and the modulated ripple to find the optimum value of G. Here, this relationship is linearly changed and Go=500 [uS] is the best correction value. Note that the conductance G shown in Eq. (7) is the theoretically reasonable equation.

As a result, the modulated ripple is reduced from 20mV to 0.8mV and the total ripple becomes 2.0 mV with the modulation signal of ±2.0V shown in Fig. 14. At the same time, the spread spectrum of the clock frequency keeps the small peak level of 0.35V against the variation of the modulation level. We have checked the effect against other frequencies and got the good results.

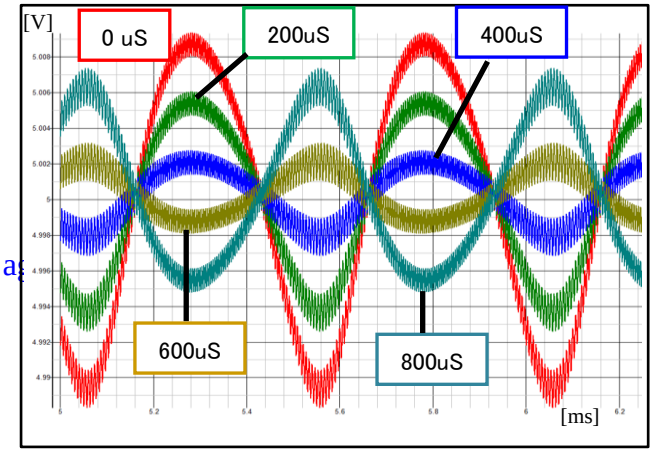

Fig. 12. Output Ripple vs. Conductance G

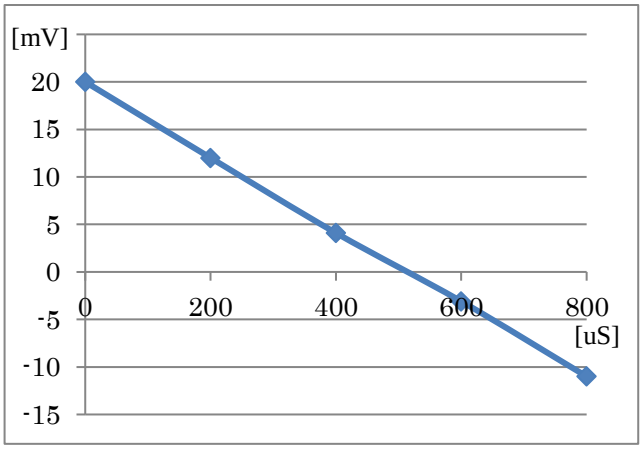

Fig. 13. Conductance G vs. Output Ripple

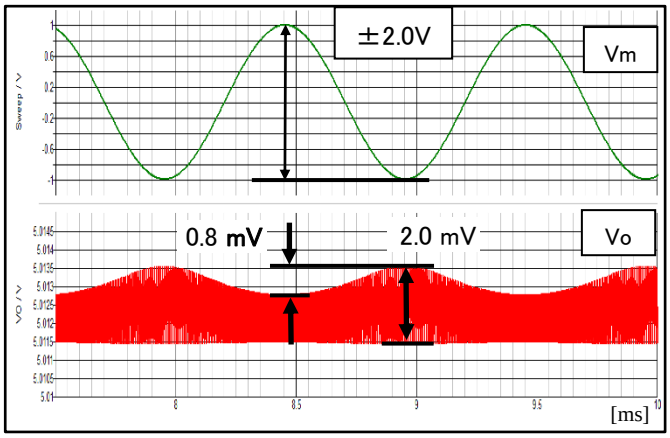

Fig. 14. Output Ripple with Correction (Vm=±2.0V, Fm=2.0 kHz)

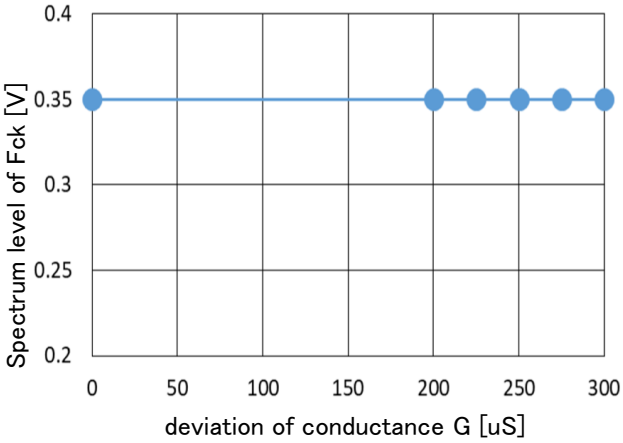

Fig. 15. Conductance G vs. Spectrum Peak (Peak Level of Clock Frequency)

4. Conclusion

We have proposed the output ripple correction method for the EMI reduction converter using the frequency modulation of the clock pulse. The output voltage ripple keeps the small level equal to that of the condition without EMI reduction. The output ripple is corrected with the compensation of the slope of the saw-tooth signal by the additional current source which relates to the modulation signal. The conductance G of the additional current source is theoretically derived with the relationship between the SAW current and the amplitude of the modulation signal.

References

[1] H. Kobayashi, T. Nabeshima,"Handbook of Power Management Circuits", ***Pan Stanford Publishers,*** 2016

[2] Y. Kobori, N. Tsukiji, N. Takai, H. Kobayashi, " EMI Reduction by Extended Spread Spectrum in Switching Converter", ***IEICE Technical Committee on Electromagnetic Compatibility Japan*** (Thailand) Jun. 2015

[3] N. Miki, K. Asaishi, N. Tsukiji, Y. Kobori, N. Takai, H. Kobayashi, " EMI Reduction Technique With Noise Spread Spectrum Using Swept Frequency Modulation for Hysteretic DC-DC Converters", ***IEEE International Symposium in Intelligent Signal Processing and Communication Systems 2017***(ISPACS2017) (Xiamen, China) Nov. 2017

[4] Y. Xiong, K. Asaishi, N. Mik i, Y. Sun, N. Tsukiji, Y. Kobori, H. Kobayashi," Multi-Phase Clock-less Switching Converter with EMI Noise Reduction", **IEICE, Circuits and Systems**, ECT-018-013 (Japanese) Mar. 2018

[5] N. Miki, T. Araii, K. Asaishi, N. Tsukiji, Y. Sun, Y. Kobori, N. Takai, H. Kobayashi," Output Voltage Ripple Compensation of Switching Converters with EMI Noise Reduction," **IEICE, Circuits and Systems**, ECT-018-026 (Japanese) Mar. 2018

[6] T. Arai, N. Mik i, Y. Sun, N. Tsukiji, Y. Kobori, N. Takai, H. Kobayashi," A Study on Ripple Compensation Switching Power Supply in EMI Reduction Method," **IEEJ,** ETG-18-80 (Japanese) Mar. 2018