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Invited

Low Switching Loss and Scalable 20-40 V LDMOS Transistors with Low Specific On-Resistance

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Abstract. This paper describes 0.18 μm CMOS compatible, low switching loss, and scalable 20-40 V dual RESURF LDMOS transistors with low specific on-resistance for automotive applications. The drift region of the proposed 40 V operation device is scaled down to get lower operation voltage devices. Simulations verified that each of the proposed devices scaled down has a wide SOA without having the drain current expansion region at the maximum rated gate and drain voltages, a state-of-the-art level characteristic of specific on-resistance $R_{on}A$ vs. breakdown voltage BV_{DS} (the 20 V operation device: $R_{on}A$ = 18.4 mΩ·mm^2 at BV_{DS} = 40 V, the 40 V operation device: $R_{on}A$ = 40.9 mΩ·mm^2 at BV_{DS} = 62 V), and a very low FOM (on-resistance × gate charge) due mainly to the grounded field plate of the proposed device (the 20 V operation device: FOM = 34.2 mΩ·nC, the 40 V operation device: FOM = 48.2 mΩ·nC which is about one-third that of a conventional device).

1. Introduction

Lateral Double Diffused MOS (LDMOS) transistors are widely used as switching devices of power converters for automotive as well as consumer applications. Automotive applications require a much wider Safe Operating Area (SOA) and higher reliability for hot carriers. In order to obtain a wider SOA, the drain Current Expansion (CE) [1,2] caused by the Kirk effect due to high drain currents has to be suppressed. In order to obtain the higher reliability, the impact ionization caused by high electric fields near the gate-side drift region edge of an LDMOS transistor has to be reduced. To meet these requirements, we proposed a 0.35 μm CMOS dual Reduced Surface Field (RESURF) 30-50 V LDMOS transistor [3,4,5]. Furthermore, the applications need much lower power dissipation (or lower heat generation). To respond to this, we also proposed a low switching loss 0.18 μm CMOS dual RESURF 40 V LDMOS transistor with low specific on-resistance [6] by improving the former 30-50 V LDMOS transistor with connecting the field plate to the ground. However, LDMOS transistors having multiple operation voltages (20-40 V) on a chip are further required to facilitate circuit design.

In this paper, we present low switching loss and scalable 20-40 V LDMOS transistors by shrinking the drift region of the 0.18 μm CMOS dual RESURF 40 V LDMOS transistor. In the following sections, the conventional and the proposed structures are introduced, and scalable device characteristics are verified using a 3D device simulator, DESSERT (Sample version) developed by AdvanceSoft Corporation [7]. Simulation results indicate that even a scaled (20 V operation) device has a wide SOA with sufficiently suppressed CE, a state-of-the-art level characteristic of specific on-resistance vs. breakdown voltage, low switching loss, and high hot carrier endurance.

2. Device structures

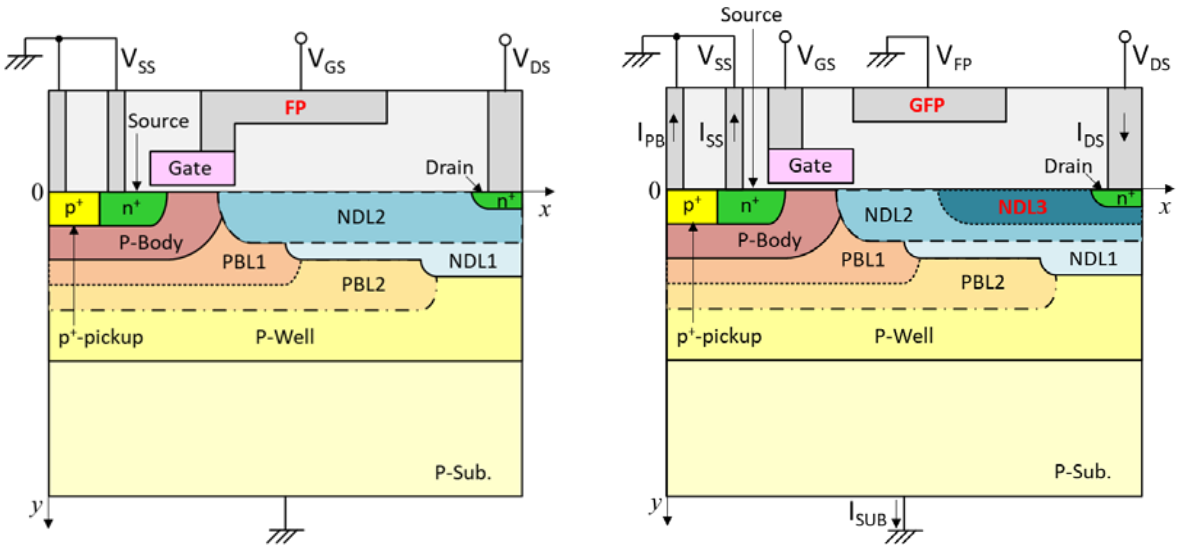
2.1 Conventional LDMOS transistor

Fig. 1 (a) shows a cross-section of the conventional 0.35 μm CMOS compatible LDMOS transistor. The conventional device has two P-type Buried Layers (PBL1 and PBL2). PBL1 enhances the RESURF effect near the gate-side drift region edge, and PBL2 contributes to the uniformity of the electric field in the drift region. PBL2 has an opening under the drain to avoid premature breakdown between the drain and the substrate. The drift region consists of two N-type Drift Layers (deep NDL1 and shallow NDL2). NDL1 is the base drift layer, and NDL2 enhances the doping concentration in the shallow drift region, leading to enlargement of the SOA due to CE suppression [8]. The Field Plate (FP) connected to the gate complements the RESURF effect, but increases the switching loss due to the Miller capacitance. Here, PBL1 and 2, and NDL1 and 2 are simply formed without affecting the thermal budget of the existing CMOS fabrication process flow.

2.2 Proposed LDMOS transistor

Fig. 1 (b) shows a cross-section of the proposed 0.18 μm CMOS compatible LDMOS transistor improved from the conventional device. The proposed device has a Grounded Field Plate (GFP) in order to reduce the Miller capacitance. However the GFP increases the on-resistance because it repels the electrons in the drift region in the on-state. In order to reduce the on-resistance, the proposed device further has an N-type Drift Layer (NDL3) in the shallow drift region except the close of the gate-side drift region. NDL3 also suppresses CE. The x-direction cell pitch of the proposed device (3.555 μm) is 0.17 μm shorter than that of the conventional device. One cell size of the proposed device for the simulation is 3.555 μm × 0.3 μm. The lengths of the drift region and the FP over the drift region of the proposed device are the same as those of the conventional device, respectively.

The proposed device is scaled down with varying the lengths of PBL1 and 2 under the drift region, and FP in proportion to the change in the drift region length (DRL). Here, the length of NDL3 is not changed to avoid an increase in the electric field near the gate-side drift region edge.



(a) Conventional LDMOS transistor (b) Proposed LDMOS transistor

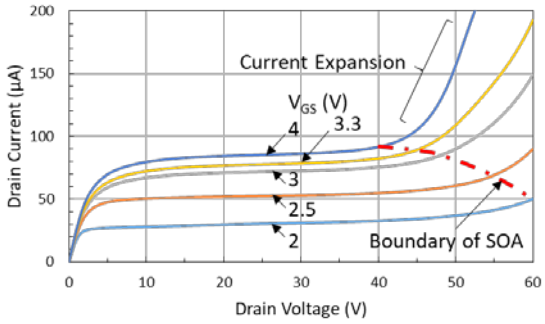
Fig. 1. Cross-sections of the conventional and the proposed LDMOS transistors.

3. Simulation results

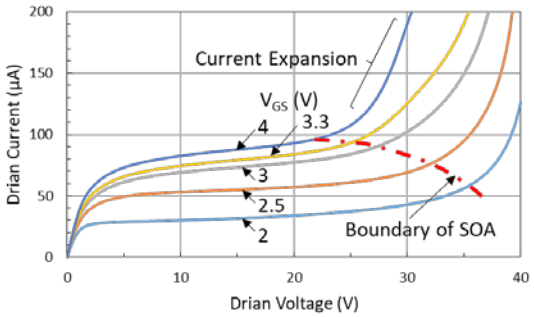
3.1 I_{DS}-V_{DS} characteristics

Fig. 2 (a) and (b) show the drain current I_{DS} vs. drain voltage V_{DS} characteristics as a function of the gate voltage V_{GS} for the proposed devices with no and 50 % DRL reductions, respectively. The values of V_{DS} at the boundary of the SOA excluding the CE region are 40 V and 22 V at a maximum rated gate voltage of 4 V for the no and the 50 % DRL reduction devices, respectively. This indicates that the no DRL reduction device has a sufficient drain operation voltage of 40 V, and the 50 % DRL reduction device, of 20 V.

The specific on-resistance $R_{on}A$ (R_{on}: on-resistance, A: one cell area) can be obtained from the linear region of an I_{DS}-V_{DS} characteristic. The values of $R_{on}A$ are 40.9 mΩ·mm^2 and 18.4 mΩ·mm^2 at an operation gate voltage of 3.3 V for the no and the 50 % DRL reduction devices, respectively.

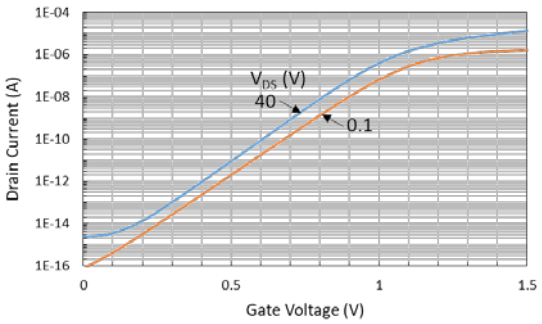


(a) No DRL reduction device
(One cell: 3.555μm×0.3μm)

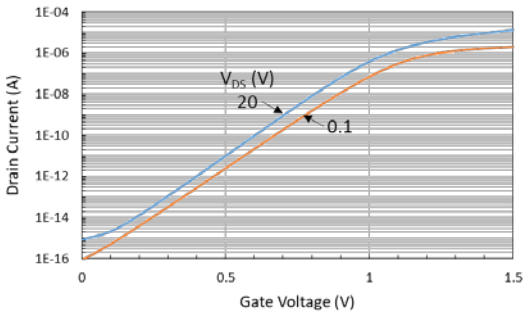


(b) 50% DRL reduction device
(One cell: 2.23μm×0.3μm)

Fig. 2. I_{DS}-V_{DS} characteristics of the proposed devices.



(a) No DRL reduction device (one cell)



(b) 50% DRL reduction device (one cell)

Fig. 3. I_{DS}-V_{GS} characteristics of the proposed devices.

3.2 I_{DS}-V_{GS} characteristics

Fig. 3 (a) and (b) show the I_{DS}-V_{GS} characteristics as a function of V_{DS} for the proposed devices with no and 50 % DRL reductions, respectively. The values of the threshold voltage V_{TH} are 1.026 V and 1.023 V at I_{DS} = 0.1 μA and V_{DS} = 0.1 V for the no and the 50 % DRL reduction devices, respectively. These V_{TH} values are almost the same. The V_{TH} shifts due to V_{DS} biases of 40 V and

20 V from 0.1 V are -0.104 V and -0.100 V for the no and the 50 % DRL reduction devices, respectively. These shifts are also almost the same. Thus both of the no and the 50 % DRL reduction devices have almost the same I_{DS}-V_{GS} characteristics at each of the V_{DS} biases, and very low leak currents.

3.4 Breakdown characteristics

Fig. 4 shows the I_{DS}-V_{DS} characteristics at V_{GS} = 0 V of the proposed devices. The values of the breakdown voltage BV_{DS} at I_{DS} = 1×10^{-13} A are 62 V and 40 V for the no and the 50 % DRL reduction devices, respectively. This indicates that the value of BV_{DS} for the no DRL reduction device is high enough for 40 V operation, and that for the 50 % DRL reduction device, for 20 V operation.

Fig. 5 (a) and (b) show the distributions of the electric field magnitude upon breakdown for the proposed devices with no and 50 % DRL reductions, respectively. High electric field locations causing breakdown are all in the bulk for the no and the 50 % DRL reduction devices, leading to less damage to the gate oxide and the surface. Therefore the proposed devices would have good Electro-Static Discharge (ESD) performance, if they are used as ESD devices with the gates grounded.

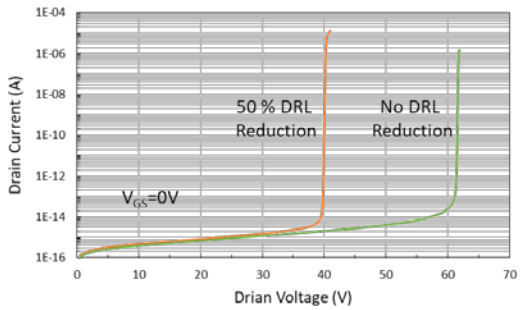


Fig. 4. Breakdown characteristics of the proposed devices (one cell).

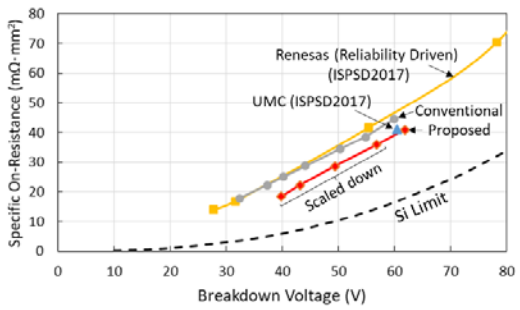
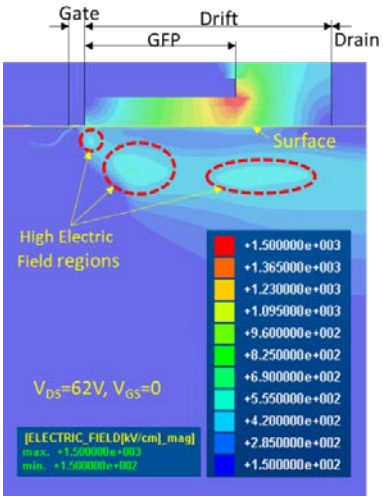
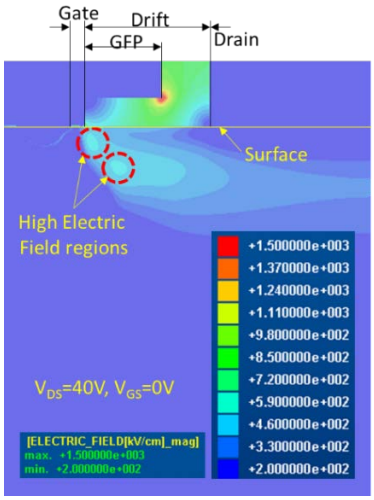


Fig. 6. $R_{on}A$ vs. BV_{DS} characteristics.



(a) No DRL reduction device



(b) 50% DRL reduction device

Fig. 5. Distributions of the electric field magnitude upon breakdown of the proposed devices.

3.5 $R_{on}A$-BV_{DS} characteristics

Fig. 6 shows the $R_{on}A$-BV_{DS} characteristics for the conventional device, the proposed device, and the state-of-the-art level devices presented by UMC Co. [9] and Renesas Semiconductor Manufacturing Co. Ltd. [10]. Fig. 6 states that the proposed device is improved from the conventional device, and is comparable with UMC's characteristic at $BV_{DS} \fallingdotseq 60$ V. This proves that the $R_{on}A$-BV_{DS} characteristics of the proposed devices including the devices scaled down are state-of-the-art level.

3.6 Hot carrier endurance

Fig. 7 shows the V_{GS} dependences on the P-body current I_{PB} plus the substrate current I_{SUB} (the hole current generated by impact ionization) for the proposed devices. Each of the characteristics has a peak near V_{GS} = 2 V due to Drain Avalanche Hot Carriers (DAHC) generated by impact ionization in the vicinity of the drain of the intrinsic MOSFET (the gate-side drift region edge) operating in the saturation mode. The peak value of the no DRL reduction device is a little bit higher than that of the 50 % DRL reduction device.

Fig. 8 (a) and (b) show the profiles of the electric field in the minus x-direction $-E_{xx}$ along the surface at V_{GS} = 2 V for the proposed devices with no and 50 % DRL reductions, respectively. Each of the electric field profiles has a peak near the gate edge (at a distance $x \fallingdotseq 1000$ nm). The peak value of the no DRL reduction device biased at V_{DS} = 40 V (the red dot in Fig. 8 (a)) is almost the same as that of the 50 % DRL reduction device biased at V_{DS} = 20 V (the red dot in Fig. 8 (b)). Furthermore, the source current I_{SS} (the electron current) of the no DRL reduction device biased at V_{DS} = 40 V (I_{SS} = 30.7 μA for one cell) is also almost the same as that of the 50 % DRL reduction device biased at V_{DS} = 20 V (I_{SS} = 30.8 μA for one cell). Since the number of the holes generated by impact ionization depends on I_{SS} and E_{xx} [11], the amount of the holes generated near the gate edge of the no DRL reduction device is almost the same as that of 50 % DRL reduction device. This states that there would be no difference between the no and the 50 % DRL reduction devices for the damage caused by the hot carriers generated near the gate edge. Since the no DRL reduction device would likely be able to have high hot carrier endurance [6], the 50 % DRL reduction device would also be able to have. The hole current difference between the no and the 50 % DRL reduction devices shown in Fig. 7 is due to the electric field profile difference in the drift region. The no DRL reduction device has another peak at $x \fallingdotseq 2700$ nm in the drift region which causes impact ionization, resulting in an increase of the hole current.

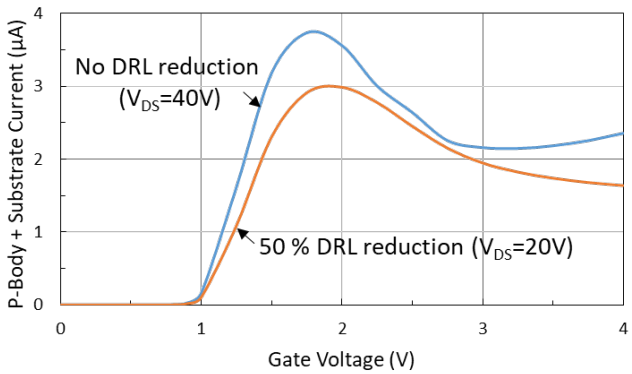
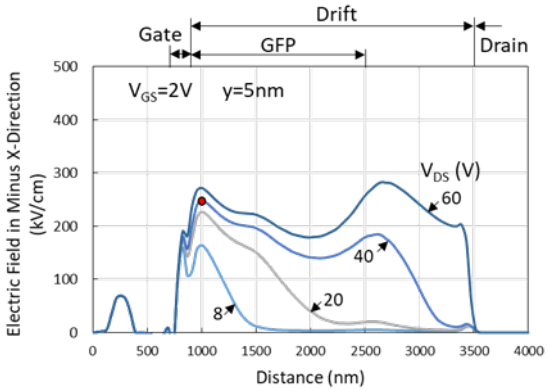
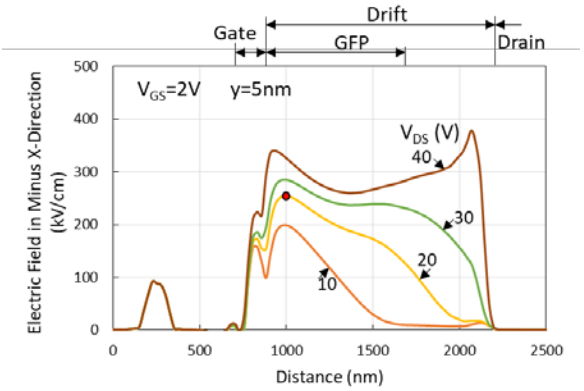


Fig. 7. V_{GS} dependences on I_{PB} + I_{SUB} (the hole current) for the proposed devices (one cell).



(a) No DRL reduction device



(b) 50% DRL reduction device

Fig. 8. Profiles of the electric field in the minus x-direction along the surface for the proposed devices.

3.7 FOM and total power dissipation

Fig. 9 shows the circuit for obtaining turn-on characteristics of the proposed devices. Time variations of the gate current and voltage during turn-on of the devices are obtained from this circuit (see Fig. 10). From Fig. 10, a value of the gate charge density Q_g/A stored in the gate capacitance during turn-on is 1.18 nC/mm^2 for the no DRL reduction device. Therefore its figure of merit (FOM) for $R_{on}Q_g$, $R_{on}A \times Q_g/A$, has a value of 48.2 mΩ·nC which is about one-third that of the conventional device [6]. As for the 50 % DRL reduction device, a value of Q_g/A is 1.86 nC/mm^2, leading to FOM = 34.2 mΩ·nC. Namely, the FOM of the 50 % DRL reduction device is about two-thirds lower than that of the no DRL reduction device. This is due to the much lower $R_{on}A$ of the 50 % DRL reduction device.

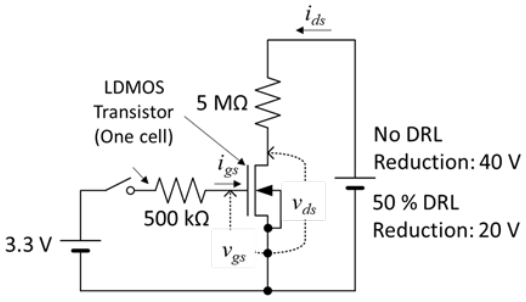


Fig. 9. The circuit used to obtain turn-on characteristics.

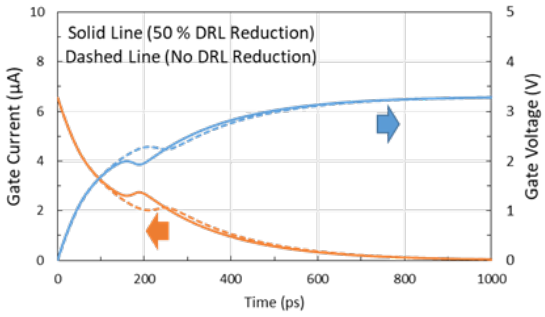


Fig. 10. Time variations of the gate current and voltage during turn-on for the proposed devices (one cell).

Table 1 shows the components of the switching loss per switching cycle E_{SW} for the proposed devices. The E_{SW} consists of the gate driving loss per switching cycle E_{GD} and the turn-on/off loss per switching cycle $E_{ON/OFF}$, where the turn-off loss per switching cycle E_{OFF} is assumed to be equaled to the turn-on loss per switching cycle E_{ON}. The E_{SW} value of the 50 % DRL reduction device is about 50 % lower than that of the no DRL reduction device. This is mainly due to the lower supply voltage for the 50 % DRL reduction device.

Fig. 11 shows the switching frequency f dependences on the total power dissipation density P_{TD} as a function of the duty ratio D_{on} for the proposed devices. The P_{TD} consists of the power dissipation density during the switching, $E_{SW} \times f$, and that during the steady state conduction depending on D_{on}. The P_{TD} of the 50 % DRL reduction device is lower than that of the no DRL reduction device for each D_{on}, and is further lower in a high switching frequency region. This is due to much lower E_{SW} and $R_{on}A$ for the 50 % DRL reduction device.

Table 1 Components of the switching loss per switching cycle for the proposed devices.

Drift Region Length	E_{GD} [J/mm^2]	$E_{ON/OFF}$ [J/mm^2]	E_{sw} [J/mm^2]
No Reduction	3.89×10^{-9}	1.91×10^{-8}	2.30×10^{-8}
50 % Reduction	6.14×10^{-9}	5.52×10^{-9}	1.17×10^{-8}

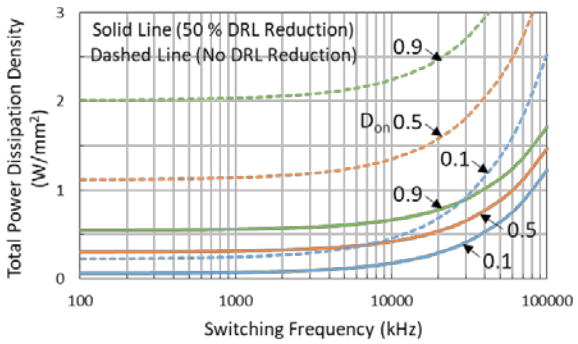


Fig. 11. Switching frequency dependences on P_{TD} for the proposed devices.

4. Conclusion

Each of the proposed 20-40 V operation LDMOS transistors has a wide SOA without having the CE region at the maximum rated gate and drain voltages, a state-of-the-art level characteristic of $R_{on}A$ vs. BV_{DS}, and a very low FOM representing high suppression of conduction and switching losses. Hot carrier endurance of the 20 V operation device would be almost the same as the 40 V operation device which would likely be able to have high hot carrier endurance. Therefore all the proposed devices can be adequately applied to harsh environment automotive applications. Furthermore, the proposed devices having different operation voltages can be made on a chip only with changing the mask layout, leading to the high flexibility of circuit design without increasing the fabrication cost.

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