***Proceedings of International Conference on Technology and Social Science 2023 (ICTSS 2023)***
***ICTSS2023-IPS02-005 (Invited Paper)***

# A Fine On-Chip Online Delay Measurement Using a MUX Chain for Failure Prediction and Analysis

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**Keywords:** on-chip online delay measurement, fine resolution, MUX chain, calibration, phase-variable PLL

**Abstract.** This paper presents a fine on-chip online delay measurement using a multiplexer (MUX) chain for enhancing reliability of logic circuits in field. The proposed method uses the secondary shadow clock with the MUX chain for fine phase shift cascaded with the conventional coarse phase-variable PLL. In the proposed method, first, we perform the coarse slack measurement of target paths based on consecutive path delay test with the forward coarse phase shifting with the phase-variable PLL clock. Second, we perform the fine slack measurement based on consecutive path delay test with the backward fine phase shifting with the MUX chain. The proposed fine and low-cost delay on-chip measurement can be used not only for online prediction of timing failures due to process, voltage, and temperature (PVT) variation and aging, but also for the precise online analysis of failure mechanisms. The experimental results with AMD Artix7 FPGA show that the measurement resolution is 10.1 ps. It is 9.7 % of the resolution of the conventional methods. The absolute values of DNL and INL are less than 0.005 LSB.

## 1. Introduction

Aggressively scaled CMOS process technologies have led to extremely fast and low power processors and SoCs for high performance handheld devices and AI accelerators. On the other hand, because timing failures caused by PVT variations and aging become serious, it is difficult to guarantee the function of a modern VLSI in field just only with offline testing before shipment. Significant research efforts have been focused on the testing for the online timing failures [1,2]. Most of them are focused on online failure prediction and analysis [3,4].

Path delay measurement is useful for both prediction and analysis. In on-chip online path delay measurement, the delay values of a set of critical paths vulnerable to timing failures are measured periodically. The time series of the measured delay data is used for timing failure prediction and analysis of failure mechanisms, such as the analysis of relations among delay degradation, workloads to the paths, and PVT variations. Various methods for delay measurement have been proposed. Online path delay measurement with a phase-shift PLL is one of them [5,6]. However, the resolution of delay measurement of this approach depends on the specification of the used PLL.

This paper presents a fine on-chip online delay measurement using a multiplexer (MUX) chain for enhancing reliability of logic circuits in field. The proposed method uses the secondary shadow clock with the MUX chain for fine phase shift cascaded with the conventional coarse phase-variable PLL. In the proposed method, first, we perform the coarse slack measurement of target paths based on consecutive path delay test with the forward coarse phase shifting with the phase-variable PLL clock. Second, we perform the fine slack measurement based on consecutive path delay test with the backward fine phase shifting with the MUX chain. The proposed fine and low-cost delay on-chip measurement can be used not only for online prediction of timing failures due to PVT variation and aging, but also for the precise online analysis of failure mechanisms.

The rest of this paper is organized as follows. Section 2 explains the proposed method. Section 3 shows the experimental results. Finally, section 4 concludes the paper.

## 2. Fine Online Delay Measurement Using a MUX Chain

This section presents the detail of the proposed method. 2.1 describes the proposed measurement architecture and the basics of slack measurement. 2.2 shows the MUX chain used for the backward fine phase shifting of the proposed slack measurement. Finally, 2.3 describes the scheme of the proposed slack measurement.

### 2.1 Architecture and Measurement

Figure 1 shows the block diagram of the proposed measurement architecture. The upper part is the circuit under measurement. This circuit consists of 4 Flip-Flops $FF_0$-$FF_3$ and a logic block. The input and the output of $FF_i$ are $D_i$ and $Q_i$, respectively. The inputs EN and CLK are the enable input and the clock input, respectively. When EN = 1, the Flip-Flops work in synchronization with CLK. When EN = 0, they keep the output values. Assuming an implementation with an AMD FPGA, all the Flip-Flops have the enable input EN. However, even when they do not have an enable input, the proposed method can be still implemented.

The signals inside the circuit propagate from left to right. Accordingly, the outputs of $FF_0$ or $FF_1$ are the start points of the paths of the circuit. The inputs of the $FF_2$ or $FF_3$ are their end points. The bold line connected the output of $FF_0$ with the input of $FF_3$ is the critical path of the circuit.

The bottom part is the circuit for the implementation of the proposed measurement. It is composed of a controller, a system clock generator, a PLL clock generator, a MUX chain, and a shadow Flip-Flop SDFF. The input of SDFF $D_s$ is connected to the end of the critical path. The proposed method measures the path whose start point is $Q_0$ and the end point is $D_s$, which includes the critical path except the segment from the fanout point to $D_3$. We call the path 'path under measurement'. The phase of the system clock CLK is fixed to 0. The phase of the PLL clock $CLK_{PLL}$ can be shifted with coarse resolution. The MUX chain is cascaded with the PLL clock generator. The output of the PLL clock generator $CLK_{PLL}$ is connected with the input of the MUX chain IN. The output of the MUX chain OUT is the shadow clock SCLK. The delay of the MUX chain from IN to OUT can be adjusted with fine resolution. Consequently, the phase of the shadow clock can be adjusted in both coarse and fine manners. The delay from IN to OUT of the MUX chain can be measured with calibration.

All the measurement sequences are controlled with the controller. The outputs of the controller synchronize with either CLK or $CLK_{PLL}$. It has the inputs TEST and TRG. When TEST = 1, the system is in measurement mode; otherwise it is in normal operation mode. The input TRG is the trigger input of path delay test. Path delay test is executed in a synchronized manner with the positive transition of TRG. The output EN of the controller controls the operation of $FF_0$- $FF_3$. The output SEN of the controller controls the operation of SDFF. The controller controls the phase of SCLK although it is omitted due to space limitation.

The proposed method measures the delay of a path with repeating Launch-on-Capture (LOC) path delay test of the path under measurement consecutively shifting the phase of SCLK. In LOC path delay test, a transition is launched at the start point of the path which is connected to an output of a Flip-Flop by applying a clock pulse in normal operation mode. The transition arrives at the input of the common shadow Flip-Flop. The path is sensitized based on single-path sensitizable criterion [7]. The shadow Flip-Flop captures the input value synchronized to SCLK. Figure 2 shows the timing chart of a path delay test for the path under measurement. When TEST = 1, EN becomes 1 for two-clock period synchronizing with the positive transition of TRG. During EN = 1, $FF_0$-$FF_3$ work in a synchronized manner with CLK. In the 1st clock inside the 1st period that EN = 1, a positive transition is launched in $Q_0$. The transition arrives at the end point of the path under measurement through the logic circuit. The input SEN becomes 1 for a clock period and the shadow Flip-Flop SDFF captures the value of the end point of the path under measurement. The timing SCLK captures the value of the end point of the path under measurement is decided with the length of the path and the range of the measurement considered. When TEST = 0, EN and SEN are fixed to 1 and 0, respectively.

The proposed online delay measurement is the foreground one that stops the normal operation temporally before delay measurement. Because it is used for timing failure prediction or analysis of delay degradation, it is enough to get the difference of delay of the path under measurement. In this paper, we do not intend to measure the absolute delay of the path, but try to measure the slack against the timing that SDFF captures the value of the end point of the target path. Figure 3 shows an example of measurement sequences. In this example, the clock period of both CLK and SCLK is T. We assume that the path under measurement is fault-free.

The proposed method measures the timing slack with repeating path delay test of the path under measurement by shifting the data capture timing of SDFF with coarse resolution and fine resolution. Let $t_s$ be the initial capture timing of SDFF. When path delay test is executed, a positive transition is launched in $Q_0$ in time 3. The transition arrives at $D_s$ just before time 8 in this example. The shadow Flip-Flop SDFF captures the value of $D_s$ at $t_s$ just before time 12.

Now we start the slack measurement. Here the slack is defined as $t_s$ minus the arrival time of transition from the start point of the path under measurement. First, path delay test is performed with the initial capture timing of SDFF $t_s$. Let the captured value be the expected value $E$. Because the arrival time of the transition is before $t_s$, $E = 1$ in this example. Second, we repeat path delay test with shifting phase of clock forward by every $2\pi\Delta T/T$ coarsely until the captured value becomes $\bar{E}$. When the clock phase is shifted by $2\pi\Delta T/T$, the capture timing is $t_s - \Delta T$. Because the transition arrives at $D_s$ before $t_s - \Delta T$, the test response is $E$. When the clock phase is shifted by $4\pi\Delta T/T$, the capture timing is $t_s - 2\Delta T$. In this case, the test response is also $E$. However, when the clock phase is shifted by $6\pi\Delta T/T$, the capture timing is $t_s - 3\Delta T$. Because the arrival time of the transition is after $t_s - 3\Delta T$, the test response is $\bar{E}$ in this case. Now we know that the slack is less than $3\Delta T$. Third, we repeat path delay test with shifting phase of clock backward by every $2\pi\Delta t/T$ until the captured value becomes $E$. When the clock phase is shifted $-2\pi\Delta t/T$, the capture timing is $t_s - 3\Delta T + \Delta t$. Because the arrival time of the transition is after $t_s - 3\Delta T + \Delta t$, the test response is $\bar{E}$. Next, when the clock phase is shifted by $-4\pi\Delta t/T$, the capture timing is $t_s - 3\Delta T + 2\Delta t$. Because the arrival time of the transition is before $t_s - 3\Delta T + 2\Delta t$, the test response is $E$. Finally, we found that the slack is $3\Delta T - 2\Delta t$. In general, the number of the forward coarse phase shift is $n$ and that of the backward fine phase shift is $m$, the slack is $n\Delta T - m\Delta t$. We let the number of the coarse phase shift $n + 1$ deliberately. As a result, the number of the backward phase shift is $m'$. Then the slack is calculated as $(n+1)\Delta T - m'\Delta t$. This yields the equation $n\Delta T - m\Delta t = (n+1)\Delta T - m'\Delta t$. This equation consequently gives

$$\Delta t = \frac{\Delta T}{m' - m} \tag{1}$$

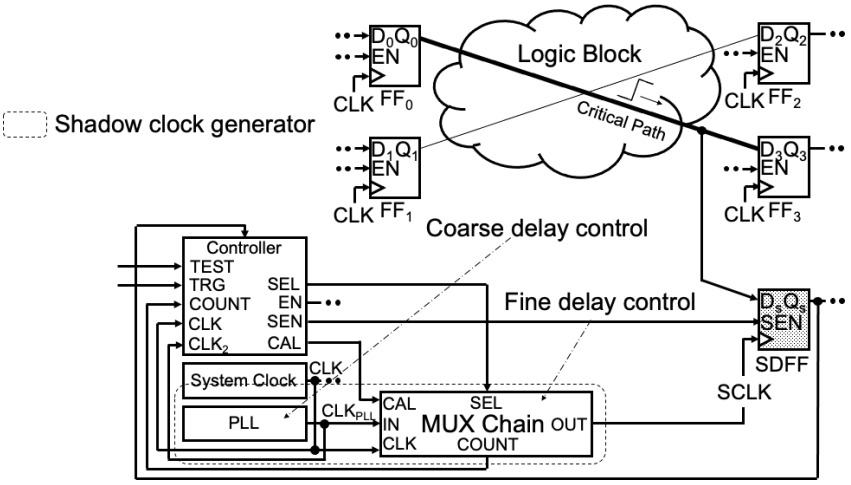


Fig. 1. Architecture of proposed online delay measurement with fine resolution.

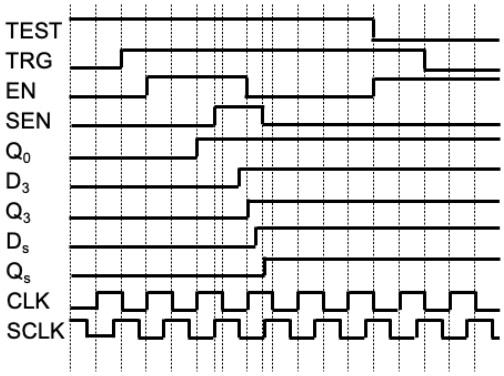


Fig. 2. Timing chart of a path delay test for proposed delay measurement.

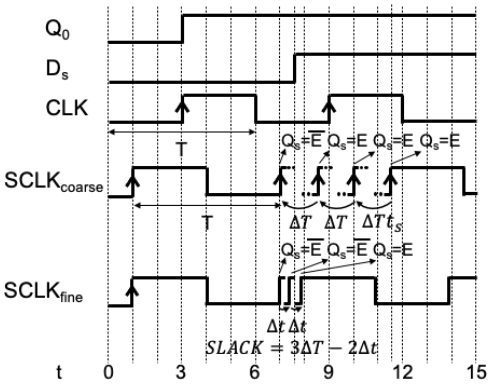


Fig. 3. Timing chart of proposed delay measurement with consecutive path delay test.

Usually, the paths under measurements are single-path sensitizable. Multiple robust sensitizable paths with common end point can be sensitized simultaneously when we want to measure the worst slack [5,7]. The measurement of what and how many paths depends on the kind of circuit and the aim of the measurement in general. For failure prediction, the set of paths are usually chosen by designers. These paths have higher workload and vulnerable to aging. Because there exist multiple end points to be observed in general, extra Flip-Flops or multiplexers to observe the end points are required. It results in extra area overhead. Therefore, designers should consider the path selection and the extra area for the measurement. As shown in the timing chart of Fig. 2, the shadow flip flops capture the test response

in the period when SEN = 1. The optimal timing to rise up SEN depends on delay of the redundant wire and the MUX chain. The timing is adjusted with the controller of Fig. 1. The measured slack may contain the effect of aging of the redundant wire. It causes false positive. We can avoid it with measurement of multiple independent paths with common aged redundant wire.

## 2. MUX Chain for Fine Phase Shift

Figure 4 illustrates the 4-stage MUX chain used for the backward fine phase shifting of the proposed slack measurement. We explain the MUX chain with this example. The clock input and the output are IN and OUT, respectively. The control input SEL controls the delay of the path between IN and OUT. The MUX chain is composed of an internal 4-stage 2-to-1 MUX chain and a redundant 2-to-1 MUX, which are serially connected. Each input of SEL is connected to the corresponding control input $S_i$ of each *i*th stage. The symbol d*i*0 is the delay of the upper input wire of the *i*th stage and d*i*1 is that of the bottom wire of the internal MUX. The input of the internal MUX chain is $IN_0$. The input $IN_0$ is also the output of the redundant MUX. The redundant MUX is controlled by the CAL input. The inverted OUT is feedback to an input of the redundant MUX. When CAL = 0, an external clock is launched from IN. When CAL = 1, a ring oscillator is constructed. The oscillation counter counts the oscillation times. The output is $COUNT_{OSC}$. The reference counter is used for calculation of the oscillation frequency of the ring oscillator whose output is $COUNT_{REF}$. The bold line is the path for the clock signal. The narrow line is redundant negative feedback path for the measurement of delay of the path for the clock signal. To make phase shift function, the fan-out routing of input wires of each 2-to-1 MUX of the internal MUX chain are routed as randomly as possible. For example, let d00, d01, d10, d11, d20, d21, d30, d31 be 0.56 ns, 0.40 ns, 0.54 ns, 0.58 ns, 0.48 ns, 0.50 ns, 0.56 ns, 0.50 ns, respectively. The delay from IN to OUT depends on the control input SEL. For example, when $S_0S_1S_2S_3$ = 0011, 0010, 0110, the propagation delay values are 2.10 ns, 2.16 ns, 2.20 ns, respectively.

When the target resolution is 50 ps, the initial phase is 2.10 ns, and the range is 100 ps, the ideal phases are 2.10 ns, 2.15 ns, and 2.20 ns, respectively. Consequently, we can perform the phase sweep up from 2.10 ns to 2.20 ns with the 50 ps resolution in 10 ps maximum phase error. This multiplexer can be used as a fine phase shifter whose resolution is about 50 ps and the range is 100 ps. As the number of the stage of the internal MUX chain increases, the resolution becomes higher and the range becomes wider because the number of paths of the MUX chain increases exponentially. In the modern VLSIs, the difference of delay specification between a real chip and the simulation is unavoidable. Therefore, we must measure the delay of the paths from IN to OUT.

We measure it constructing the ring oscillator including the path. When CAL = 1, a ring oscillator composed of the path from IN to OUT (bold line) and a redundant path (narrow line) is constructed. By measuring the oscillation frequency, we can get the approximated delay of the path.

First, we count the time that the ring oscillator oscillates with the reference counter. When the time is $COUNT_{REF}$ and the oscillation times of the ring oscillator is $COUNT_{OSC}$, the oscillation period of the ring oscillator $T_{OSC}$ is $(COUNT_{REF}/COUNT_{OSC}) \cdot {f_{REF}}^{-1}$, where $f_{REF}$ is the clock frequency of the reference counter. Let t_sim(SEL) be the simulated delay of the path from IN to OUT when the control input is SEL. Let $t_{fb}$_sim be the simulated delay of the redundant feedback path including inverter and redundant MUX delay. When the difference of the delay from IN to $IN_0$ from the delay from another input of the redundant MUX to $IN_0$ is negligible, $t_{MUXC}$(SEL), which is the delay from IN to OUT when the control input of the MUX chain is SEL, can be expressed as following formula.

$$t_{MUXC}(SEL) = \frac{t\_sim(SEL)}{t\_sim(SEL)+t_{fb}\_sim} \cdot T_{OSC} = \frac{1}{1+t_{fb}\_sim/t\_sim(SEL)} \cdot \frac{COUNT_{REF}}{COUNT_{OSC}(SEL)} \cdot {f_{REF}}^{-1} \quad (2)$$

where $COUNT_{OSC}$(SEL) is the value of $COUNT_{OSC}$ after calibration when the control input of the MUX chain is SEL. The values t_sim(SEL) and $t_{fb}$_sim are obtained from the post layout simulation. Fabricated chips have both die-to-die variation and within-die variation. However, because the area of

MUX chain is small, within-die variation does not affect the ratio $t_{fb}$_sim /t_sim (SEL) of (2) very much. Die-to-die variation also does not affect the ratio very much because $t_{fb}$_sim /t_sim (SEL) is the ratio of two paths inside a small circuit. Consequently, the calculated value $t_{MUXC}(SEL)$ is robust to process variations.

To sweep up the phase with the MUX chain, the appropriate control input sequence should be applied. Here the number of the stages of the MUX chain is assumed to be N. Let $SEL'_K$ $(0 \leq K < M)$ be the *K*th control input in phase sweep up with resolution $\Delta t$. In this case, $SEL'_K$ $(0 < K < M)$ is a SEL that $|t_{MUXC}(SEL) - (t_{MUXC}(SEL'_0) + K\delta t)|$ is minimum in the set of SEL, where $SEL'_0$ is an arbitrary SEL that gives the initial phase and the variable $\delta t$ is the target time step of the delay of the MUX chain for the phase shift up. Ideally, it is equal to the fine resolution $\Delta t$. However, an oscillation counter is connected to the ring oscillator for the calibration. It works as a load during the oscillation. Consequently, the oscillation period is slightly different from that without the oscillation counter. Accordingly, $t_{MUXC}(SEL)$ calculated with (2) is slightly slower than the true value. It yields the slight difference between $\delta t$ and $\Delta t$.

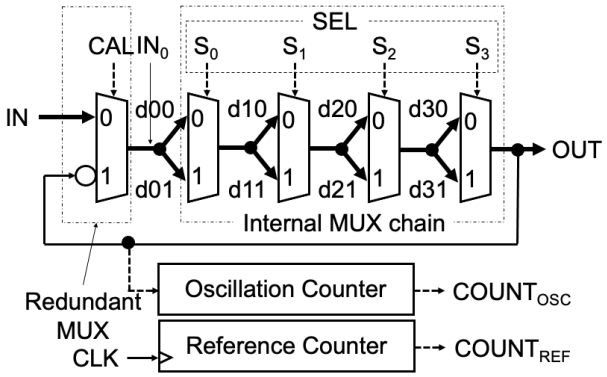


Fig. 4. 4-stage MUX chain for fine phase shift.

### 2.3 Scheme of Proposed Online Delay Measurement

The proposed online slack measurement scheme is as follows.

Step 1. Execute path delay test with the initial capture timing of SDFF and get the expected value $E$ and initialize *m* and *n* to zero.
Step 2. Shift phase forward by $2\pi\Delta T/T$ and increment *n*.
Step 3. Execute path delay test.
Step 4. If test response is equal to $\bar{E}$, go to Step 5, otherwise go to Step 2.
Step 5. Shift phase backward by $2\pi\Delta t/T$ and increment *m*.
Step 6. Execute path delay test.
Step 7. If the test response is equal to $\bar{E}$ go to Step 5, otherwise the slack is $n\Delta T - m\Delta t$.

## 3. Experimental Results

On AMD Artix7 on Digilent Basys3, we implemented the proposed method to the full-scanned s9234, which is an ISCAS89 benchmark circuit. We measured the slack of the single-path sensitizable path which has the maximum unit delay. A shadow Flip-Flop was added to observe the end point of the path. The LOC test pattern for the path delay test was generated with an in-house ATPG. The test pattern was applied from a softcore MicroBlaze to the circuit through the single scan chain. We used Vivado v2023.1 and Vitis v2023.1 for the implementation. The external oscillator MicroChip DSC1033 sent 100 MHz clock signal to the circuit. The RMS jitter of the clock signal was 12.8 ps at

100 MHz [8]. Figure 5 depicts the experimental environment. For precise evaluation, the resolution of the coarse phase shift was rather higher. The coarse phase shift function was implemented with the cascaded 8 IDELAYs. The reference clock frequency of the IDELAYs was 300 MHz to set the average tap delay 52 ps [9]. In this evaluation, the average tap delay was assumed to be the true tap delay. In this case, the range of variable delay of the IDELAY chain was 19.3 ns. Considering the typical phase resolution of the PLL on AMD FPGAs, the forward coarse phase shift resolution $\Delta T$ was set to 104 ps which is the delay of 2 taps. As the clock period of the clock signal was 10 ns, the region of the range of the IDELAY chain 9.3 ns – 19.3 ns was used. The number of the stage of the MUX chain for the fine phase shift was 16. The calibration time was 8,192 clocks. Table 1 shows the wire delay of the 16-stage MUX chain obtained from the post layout simulation. According to the simulation result, the minimum delay was 11.9 ns, the maximum delay was 14.2 ns, and the difference was 2.3 ns.

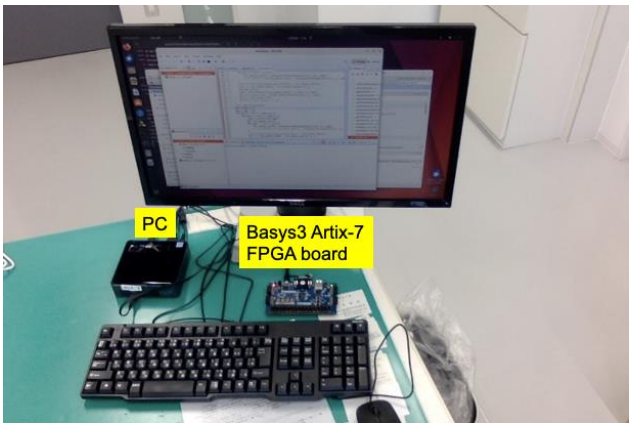


Fig. 5. Experimental environment: Basys3 Artix-7 FPGA board and PC.

Table 1. Wire delay of each stage of 16-stage MUX chain d*ij* (ps).

| *j* \ *i* | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 953 | 975 | 779 | 892 | 596 | 975 | 779 | 892 | 707 | 975 | 778 | 892 | 596 | 975 | 778 | 892 |
| 1 | 827 | 869 | 948 | 605 | 707 | 774 | 948 | 718 | 826 | 774 | 843 | 718 | 707 | 869 | 843 | 718 |

### 3.1 Resolution

We calculated the set of SEL' for the backward fine phase shift when $\delta t = 50$ ps and 100 ps, respectively. Before the calculation, the smallest 100 samples, and the largest 100 samples were removed to keep the linearity. From the remaining SEL set, we obtained the sets of SEL' and calculated $\Delta t$s from (1). The clock signal contained 12.8 ps RMS jitter. To remove the jitter, we measured $\Delta t$ 2,048 times consecutively and calculated the average value of them. We regard it as the pseudo-true $\Delta t$. Table 2 shows the result. When $\delta t = 50$ ps, $\Delta t = 10.1$ ps. It is 9.7 % of $\Delta T$ which is equal to the resolution of the conventional method in this evaluation. According to [3,4], this resolution is enough for detection and analysis of aging phenomena.

### 3.2 Linearity

We evaluated the linearity of the backward fine phase shift. In general, the differential non-linearity at digital code $k$ $DNL(k)$ when the resolution is $\tau$ is given by $DNL(k) = 1 - \frac{\Delta\tau_k}{\tau}$. In case of the proposed MUX chain, $\tau = \delta t$ and $\Delta\tau_k = t_{MUXC}(SEL'_k) - t_{MUXC}(SEL'_{k-1})$. Therefore, $DNL(k)$ is given by

$$DNL(k) = 1 - (t_{MUXC}(SEL'_k) - t_{MUXC}(SEL'_{k-1}))/\delta t \quad (3)$$

The integral non-linearity at digital code $k$ $INL(k)$ is given by

$$INL(k) = \sum_{l=1}^{k} DNL(l) \quad (4)$$

Table 3 shows the evaluation result of the DNL and INL. When $\delta t = 50$ ps, the minimum/maximum DNL are -0.0047/0.0039 LSB, respectively. The minimum/maximum INL are 0.000014/0.0047 LSB, respectively. When $\delta t = 100$ ps, the minimum/maximum DNL are -0.0022/0.0023 LSB, respectively. The minimum/maximum INL are 0.000029/0.0023 LSB, respectively. Consequently, the absolute values of DNL and INL of the proposed fine phase shift is less than 0.005 LSB.

Table 2. Resolution of backward fine phase shift $\Delta t$ (ps).

| $\delta t$ (ps) | $\Delta t$ (ps) | $\Delta T$ (ps) | $\Delta t/\Delta T$ (%) |
|---|---|---|---|
| 50 | 10.1 | 104 | 9.7 |
| 100 | 24.2 | 104 | 23.3 |

Table 3. DNL and INL of backward fine phase shift (LSB).

| $\delta t$ | $\Delta t$ | DNL (LSB) | | INL (LSB) | |
|---|---|---|---|---|---|
| | | min | max | min | max |
| 50 | 10.1 | -0.0047 | 0.0039 | 0.000014 | 0.0047 |
| 100 | 24.2 | -0.0022 | 0.0023 | 0.000029 | 0.0023 |

### 3.3 Precision of Measurement

Averaging with multiple measurements reduces jitters in the measurement system. Here, we evaluated the effect of the averaging on the precision of the measurement. We measured the slack of the path 2,048 times. We regarded the average of them as the pseudo-true slack. We measured the slack and the averaged slack with 2, 4, 8, 16, and 32-time measurements 32 times respectively, and calculated the $\sigma$s in all the cases. The fine resolution $\Delta t$ was set to 10.1 ps. Figure 6 plots them. The horizontal axis is the number of measurements to get the averaged $\sigma$. The vertical axis is the averaged $\sigma$ (ps). The $\sigma$ decreases as the number of the measurement increases. To let $3\sigma$ be less than $\Delta t$, more than 4 times measurements for averaging are required.

## 4. Conclusions

This paper has presented a fine on-chip online delay measurement using a MUX chain for reliability of logic circuits after shipment. In the proposed method, a simple logic circuit for fine delay measurement is added to the conventional path delay measurement with phase-shift PLL to realize fine delay measurement. We confirmed that the proposed method realizes fine resolution in the order of 10 ps. It is about 10 % of the resolution of the conventional methods. The absolute values of DNL and INL are less than 0.005 LSB. They are enough to detect and analyze aging phenomena which occurs inside the logic circuits of modern VLSIs.

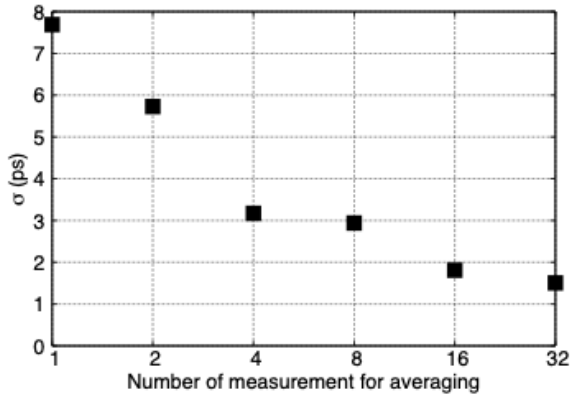


Fig. 6. Effect of averaging on $\sigma$ of measurement result.

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